C-DAC &Gujarat Technological University M.E. Electronics & Communication Engineering (VLSI & Embedded Systems Design) Gandhinagar

Semester –III
(Elective – IV & V)

2735202: Standard Cell Library and Memory Design

UNIT I– Introduction
IC design flows. Use of standard cell elements vs. custom design and Gate array paradigms. Introduction to memory types and construction of memory elements.

UNIT II - Standard cell library composition and usage
Types of standard cell elements. Logical and functional elements, primitives and complex macros. Sequential elements and register files. (Flip flop and latch design). Data path elements. Library size vs. usage in standard flows. Drive strength and cell families. Layout of library elements – single height, double height cells. Power Management cells.

UNIT III - Standard cell characterization
Usage of standard cells by various tools. Information needed at each stage of design flow. Characterization parameters, setup and runs across PVT corners. Library representation formats. (Gate level simulation, synthesis, timing, layout, timing, LVS, DRC)

UNIT IV - Memory elements and array design
Volatile and Non-volatile RAM, ROM, EPROM, Flash (EEPROM), OTP elements and cell design. State retention volatile memories. Array design – architecture, bitline/wordline optimization, sense-amps and mux/demux architecture. Memory banking, refresh cycle management. Multi-port memories. Cache memories. Special memories such as CAMs.

UNIT V– Memory defects, failures and testing, layout and characterization
Memory defects and repair. Temporal failures, Soft errors, Membist and other test techniques for memories. Memory layout and its impact on performance. Characterization of memories – timing, area, power parameters. Layout views – hard macro representation, keep outs and congestion impact.

Lab :
Tools used during laboratory works: EDA tools using Synopsys EDK 90nm library. Study and implementation of standard cell library element. Study and implementation of small register file from standard cell. Study and implementation of memory element (SRAM 6 T cell). Study and implementation of memory array (SRAM)

References:
Standard cell and memory library documentation by Vendors 90nm EDK library