# C-DAC &Gujarat Technological University M.E. Electronics & Communication Engineering (VLSI & Embedded Systems Design) Gandhinagar

**Semester –III**

**2735203:Verification Methodology**

**UNIT – I: System Verilog understanding**
Data types, Attributes, Procedural Statement, Control flow, Operators & Expressions Process, Task & Functions, Classes & OOP concepts, Random generation, constrains, Inter process communication, Clocking blocks, Programming blocks, Assertions, Its use in Design and Verification, Functional Coverage, Direct Programming Interface, Verification Using System Verilog.

**UNIT – II: Verification Using System Verilog**
What is the Functional Verification, What is the Assertion based Verification, Why use System Verilog for Verification, OOP concept for System Verilog, Layered approach for Verification, Designing with OOP, OOP classes, OOP connections, Block level testing using OOP, Chip Level Testing, Functional Coverage, Assertion Based verification, Interfacing with C

**UNIT – III: Universal Verification Methodology Understanding**
Verification Component Overview, Transaction Level Modeling (TLM), Developing Reusable Verification Component, Using Verification component, Using Register Layer Class

**UNIT – IV: Low Power Verification Techniques ( CPF/UPF)**
Need of Power Aware Simulation, Understanding Unified Power Format file, Writing CPF/UPF, Assertions checking for the low power Simulation

**UNIT – V: Verification of SOC with ARM/MIPS Processor**
ARM architecture as covered in Embedded classes, Development of ARM/MIPS BFM. Writing C test case on ARM, Using ARMCC and ARMSS compiler and linking it with simulator

**UNIT – VI: Verification Environment build and Automation.**
Use of Make file, Perl & TCL script in running the test, Running Regression of the test suit for the Device Under test, Automatic regression results generation, Merging of the code & functional coverage, Ranking of the test suit.

**References:**


1.System Verilog LRM
2.Hardware Verification with System Verilog- Mike Mintz & Robert Ekendahl System Verilog for Verification – Chris Spear
3.UVM user Manual