GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. Embedded Systems (Branch Code - 54)

Year – I (Semester – I) (W.E.F. July 2013)

Subject: Advanced Digital Circuit Design (715404) Major Elective -I

Sr. No.	Course Content	Hours
1	Overview of Digital design with Verilog: Hierarchical modeling, Number specification, data types, Operator types, Modules and Ports, Gate level modeling, Data Flow Modeling, Behavioral Modeling, Tasks and Functions, Modeling Techniques, Logic Synthesis, Verification Techniques	**15**
2	Basics of Sequential and Combinational logic circuits, Two-level and multi-level logic optimization of combinational circuits, state assignment of finite state machines.	**10**
3	Technology mapping for FPGAs, Techniques for partitioning, floor planning, placement and routing, Architectural models, scheduling, allocation and binding for high-level synthesis, Hardware-software co design, Test generation, fault simulation, built-in self-test, test structures.	**15**

Reference Books:

1. Contemporary Logic Design, Second Edition, Author: R. H. Katz, Publisher: Addison-Wesley.
2. Verilog Hdl: A Guide to Digital Design and Synthesis, Second Edition, Author: Samir Palnitkar Publisher: Pearson
3. Verilog HDL Synthesis: A Practical Primer, First Edition, Author: J. Bhasker, Publisher: Star Galaxy Publication