GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering (VLSI System Design)

Semester – III

Subject Code: 734203

Subject Name: High Speed CMOS VLSI Circuit (Major Elective -IV)

Sr. No.	Course Content
1	**Introduction:** Impact of scaling on High Speed VLSI Circuit, Inter-Die Variation, Intra-Die Variation, Fail Causes.
2	**Circuit Modeling for High Speed Design:** Simple Model: The Elmore's model Complex model: The FAST model, Delay estimation, Power Estimation
3	**Design Styles for High Speed VLSI :**Clocked Logic Styles, Non- Clocked Logic Styles, Single-Rail Domino Logic, Dual-Rail Domino Structure, Latched Domino Structure, Clocked Pass gates Logic, Static CMOS.
4	**Latching Strategies:** Basic Latch Design, Latching single-ended logic and Differential Logic, Race Free latches for Pre-charged Logic.
5	**Optimization Techniques for High Speed VLSI:** Mathematic Optimization, Circuit optimization, CAD tool for optimization.

Text/Reference:

1. Kerry Bernstein & et. al., High Speed CMOS Design Styles, Kluwer, 1999.

2. Ivan Sutherland, Bob Pproull, David Harris, Logical Efforts Designing Fast CMOS Circuits, Kluwer, 1999.

3. Jan M. Rabaey, et all: Digital Integrated Circuit: A Design perspective, second edition, 2003.

4. Design and optimization techniques of high-speed VLSI circuits by Marco Delaurenti, Phd Dissertation, December 1999.