GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Semester: III

Instrumentation & Control Engineering

(Applied Instrumentation)

Subject Name: **VLSI Design (Major Elective – IV)**

Sr. No.	Course Content
1.	**Introduction of Hardware Description Language(HDL) :** History, Concept of HDL**,** Existing Languages**, Comparison, Introduction of Verilog HDL & VHDL,** origins of VHDL,VHDL basics, Benefits of VHDL, VHDL levels of abstraction, system design flow, The VHDL design flow, Modeling hardware in VHDL, VHDL design entities, Entity declarations, Architectures.
2.	**Programming with Verilog HDL:** Verilog HDL History, framing Verilog Concepts, Hierarchy, Identifiers, White Space, Comments, Numbers, Text Macros, Modules, Semicolons, Value set, Strengths, Numbers, values and unknowns. Operators, User defined (UDP), **Conditional** statements, Task & Functions, Compiler Directive, Looping statements, State Machines.
3.	**Modeling:** Structural Model, Data Flow and Behavioral model, Efficient & Standard Coding/Commenting styles during Verilog HDL Design editing: Actual coding for module: Module definition, Parameter declaration, input output definition, register wire definition, local declaration, Assign statements, Always statements.
4.	**Designing with Digital circuits:** Combinational, Sequential, Synchronous and Asynchronous Circuits like Binary/BCD Adders and Binary Subtractors, Comparators, Multiplexers, Demultiplexer, Encoder and Decoders, Enable / Disable Inputs, Combinational PLDs, Flip-Flops, Design of Counter and ALU. Finite State Machines, Designing State Machines , Mealy and Moore Machines.
5.	**Design with Memories:** Read Only Memories, Basic ROM Structure, NOR Implementation, Distributed Gates, Array Programmability, Memory View, ROM Variations–PROM, EPROM, EEPROM, Flash Memory, Programmable Logic Arrays Structure.

6.	**Design with CPLDs and FPGAS:** Generic PLD Architecture, Complex Programmable Logic Devices, Logic Array Blocks, Macrocells, Programmable Interconnect Array, I/O Control Blocks. CPLD Architecture Description, Function Block, Advanced Interconnect Matrix (AIM), I/O Block, Output Banking. Generic FPGA Architecture, Architectural Overview, Configuration, I/O Capabilities, Program design flow, Device Programming, Design implementation using CPLD and FPGA, Simulation, Compilation. Floor planning and architecture design: floor planning methods, off-chip connections, High-level synthesis, Architecture testing.

Text Book:

1. Verilog HDL by Samir Palniker.
2. Digital Design &Implementation with Field Programmable Devices by Zainalabedin Navabi
3. The Digital Consumer Technology Handbook:- A Comprehensive Guide to Devices, Standards, Future Directions, and Programmable Logic Solutions by Amit Dhir, Xilinx, Inc.
4. Digital Electronics with PLD Integration by Nigel P. Cook.
5. Programmable Logic Design Quick Start Hand Book by Karen Parnell & Nick Mehta.
6. Programmable Logic Handbook: PLDs, CPLDs, and FPGAs by Ashok K. Sharma.
7. Spartan, 3 Platform FPGA Handbooks by Marc Baker, Kim Goldblatt, Steven Knapp.