ANALOG LOW NOISE AMPLIFIER CIRCUIT DESIGN AND OPTIMIZATION

A Thesis submitted to Gujarat Technological University

for the Award of

Doctor of Philosophy

in

Electronics & Communication Engineering

by

Hasmukh Pitambarbhai Koringa

[119997111005]

under supervision of

Dr. Vipul A Shah

GUJARAT TECHNOLOGICAL UNIVERSITY AHMEDABAD

[May – 2017]

ANALOG LOW NOISE AMPLIFIER CIRCUIT DESIGN AND OPTIMIZATION

A Thesis submitted to Gujarat Technological University

for the Award of

Doctor of Philosophy

in

Electronics & Communication Engineering

by

Hasmukh Pitambarbhai Koringa

[119997111005]

under supervision of

Dr. Vipul A Shah

GUJARAT TECHNOLOGICAL UNIVERSITY AHMEDABAD

[May – 2017]

DECLARATION

I declare that the thesis entitled **Analog Low Noise Amplifier Circuit Design and Optimization** submitted by me for the degree of Doctor of Philosophy is the record of research work carried out by me during the period from **September 2011** to **May 2017** under the supervision of **Dr. Vipul A Shah** and this has not formed the basis for the award of any degree, diploma, associateship, fellowship, titles in this or any other University or other institution of higher learning.

I further declare that the material obtained from other sources has been duly acknowledged in the thesis. I shall be solely responsible for any plagiarism or other irregularities, if noticed in the thesis.

Signature of Research Scholar: Date: 10/05/2017

Name of Research Scholar: **Hasmukh Pitambarbhai Koringa**

Place: Ahmedabad

CERTIFICATE

I certify that the work incorporated in the thesis **Analog Low Noise Amplifier Circuit Design and Optimization** submitted by Shri **Hasmukh Pitambarbhai Koringa** was carried out by the candidate under my supervision/guidance. To the best of my knowledge: (i) the candidate has not submitted the same research work to any other institution for any degree/diploma, Associateship, Fellowship or other similar titles (ii) the thesis submitted is a record of original research work done by the Research Scholar during the period of study under my supervision, and (iii) the thesis represents independent research work on the part of the Research Scholar.

Signature of Supervisor: Date: 10/05/2017

Name of Supervisor: **Dr. Vipul A Shah**

Place: Ahmedabad

Originality Report Certificate

It is certified that PhD Thesis titled **Analog Low Noise Amplifier Circuit Design and Optimization** submitted by **Mr. Hasmukh Pitambarbhai Koringa** has been examined by us. We undertake the following:

a. Thesis has significant new work / knowledge as compared already published or are under consideration to be published elsewhere. No sentence, equation, diagram, table, paragraph or section has been copied verbatim from previous work unless it is placed under quotation marks and duly referenced.
b. The work presented is original and own work of the author (i.e. there is no plagiarism). No ideas, processes, results or words of others have been presented as Author own work.
c. There is no fabrication of data or results which have been compiled / analysed.
d. There is no falsification by manipulating research materials, equipment or processes, or changing or omitting data or results such that the research is not accurately represented in the research record.
e. The thesis has been checked using **https://turnitin.com** (copy of originality report attached) and found within limits as per GTU Plagiarism Policy and instructions issued from time to time (i.e. permitted similarity index <=25%).

Signature of Research Scholar: Date: 10/05/2017

Name of Research Scholar: **Hasmukh Pitambarbhai Koringa**

Place: Ahmedabad

Signature of Supervisor: Date: 10/05/2017

Name of Supervisor: **Dr. Vipul A Shah**

Place: Ahmedabad

Copy of Originality Report

Turnitin Originality Report

Processed on: 12-Sep-2016 15:06 IST
ID: 704098353
Word Count: 27025
Submitted: 1

Ph.D. Thesis by Hasmukh P Koringa By GCET 011

Document Viewer

Similarity Index
6%

Similarity by Source

Internet Sources:	2%
Publications:	5%
Student Papers:	1%

1% match (publications)
Koringa, Hasmukh P, Bhushan D. Joshi, and Vipul Shah. "High power gain low noise amplifier design for next generation 1–7GHz wideband RF frontend RFIC using 0.18µm CMOS", 2015 19th International Symposium on VLSI Design and Test, 2015.

1% match (publications)
Arshad, S., F. Zafar, R. Ramzan, and Q. Wahab. "Wideband and multiband CMOS LNAs: State-of-the-art and future prospects", Microelectronics Journal, 2013.

1% match (Internet from 24-May-2016)
https://ecommons.usask.ca/bitstream/handle/10388/ETD-2013-12-1337/ZHANG-DISSERTATION.pdf?isAllowed=y&sequence=4

1% match (publications)
Galal, A.I.A.. "High linearity technique for ultra-wideband low noise amplifier in 0.18@mm CMOS technology", AEUE - International Journal of Electronics and Communications, 201201

1% match (Internet from 19-May-2010)
http://dspace.uta.edu

1% match (publications)
Koringa, Hasmukh P, and Vipul A Shah. "Design and optimization of narrow band low noise amplifier using 0.18µm CMOS", 2015 International Conference on Communication Networks (ICCN), 2015.

1% match (publications)
SpringerBriefs in Electrical and Computer Engineering, 2015.

PhD THESIS Non-Exclusive License to GUJARAT TECHNOLOGICAL UNIVERSITY

In consideration of being a PhD Research Scholar at GTU and in the interests of the facilitation of research at GTU and elsewhere, I, **Hasmukh Pitambarbhai Koringa** having Enrollment No. **119997111005** hereby grant a non-exclusive, royalty free and perpetual license to GTU on the following terms:

a) GTU is permitted to archive, reproduce and distribute my thesis, in whole or in part, and/or my abstract, in whole or in part (referred to collectively as the "Work") anywhere in the world, for non-commercial purposes, in all forms of media;

b) GTU is permitted to authorize, sub-lease, sub-contract or procure any of the acts mentioned in paragraph (a);

c) GTU is authorized to submit the Work at any National / International Library, under the authority of their "Thesis Non-Exclusive License";

d) The Universal Copyright Notice (©) shall appear on all copies made under the authority of this license;

e) I undertake to submit my thesis, through my University, to any Library and Archives. Any abstract submitted with the thesis will be considered to form part of the thesis.

f) I represent that my thesis is my original work, does not infringe any rights of others, including privacy rights, and that I have the right to make the grant conferred by this non-exclusive license.

g) If third party copyrighted material was included in my thesis for which, under the terms of the Copyright Act, written permission from the copyright owners is required, I have obtained such permission from the copyright owners to do the acts mentioned in paragraph (a) above for the full term of copyright protection.

h) I retain copyright ownership and moral rights in my thesis, and may deal with the copyright in my thesis, in any way consistent with rights granted by me to my University in this non-exclusive license.

i) I further promise to inform any person to whom I may hereafter assign or license my copyright in my thesis of the rights granted by me to my University in this non-exclusive license.

j) I am aware of and agree to accept the conditions and regulations of PhD including all policy matters related to authorship and plagiarism.

Signature of Research Scholar: _____

Name of Research Scholar: **Hasmukh Pitambarbhai Koringa**

Date: 10/05/2017 Place: Ahmedabad

Signature of Supervisor:_____

Name of Supervisor: **Dr. Vipul A Shah**

Date: 10/05/2017 Place: Ahmedabad

Seal:

Thesis Approval Form

The viva-voce of the PhD Thesis submitted by Shri **Hasmukh Pitambarbhai Koringa** (En. No. **119997111005**) entitled **Analog Low Noise Amplifier Circuit Design and Optimization** was conducted on 10/05/2017 (Wednesday) at Gujarat Technological University.

(Please tick any one of the following option)

The performance of the candidate was satisfactory. We recommend that he be awarded the Ph.D. Degree.

Any further modifications in research work recommended by the panel after 3 months from the date of first viva-voce upon request of the Supervisor after which viva-voce can be re-conducted by the same panel again.

(briefly specify the modifications suggested by the panel)

The performance of the candidate was unsatisfactory. We recommend that he should not be awarded the Ph.D. Degree.

(The panel must give justifications for rejecting the research work)

Name and Signature of Supervisor with Seal

---

1) (External Examiner -1) Name and Signature

---

2) (External Examiner -2) Name and Signature

---

3) (External Examiner -3) Name and Signature

ABSTRACT

The design of RF frontend for the next generation wireless communication is one of the emerging areas of research in field of RFIC. In 2002 Federal Communication Committee (FCC) had released 3.1 - 10.6 GHz Ultra Wideband (UWB) for commercial purpose with two restriction, low power transmission (Emission Isotropic Radiated Power must be lower then -41.3 dBm/MHz) and 500 MHz minimum bandwidth. These restrictions put stringent requirements on designing of UWB receiver. Overall sensitivity and noise figure of receiver is dominated by the first amplifier block of receiver known as Low Noise Amplifier (LNA). Due to very large 7.5 GHz wide bandwidth UWB technology has desirable features such as less multipath fading, good range and time resolution, high data rate and easier material penetration. The UWB technology is widely use in image penetration, high data rate short distance wireless communication, high accuracy locating and positioning and medical applications. Most challenging task in implementation of UWB technology is to design LNA for UWB receiver. Realization of UWB receiver requires wideband matching, high power gain, low noise figure and good linearity LNA.

In this thesis proposed design of 3.1 - 10.6 GHz wideband high power gain Low Noise Amplifier for UWB receiver. Common Gate (CG) configuration of amplifier is used in the first stage of UWB LNA design for wideband input impedance matching. Input impedance and Noise Figure (NF) of the CG are analyzed and optimized to improve performance of the LNA. The gain of design is improved by using cascode Common Source (CS) stages after CG. NF and power gain of the design are improved by using inductive load in each stage. Overall wideband high flat gain is achieved by resonate each stage parallel tune circuit at different frequencies of interested band. This novel multistage UWB LNA design provides very high power gain, low noise figure, wideband input impedance matching and good linearity in interested 3.1 – 10.6 GHz wideband.

Simulated results shows the proposed high power gain UWB LNA design has 20-30 dB power gain and 2.8-6 dB NF in interested band. The design achieved input impedance match (S_{11}) and linearity measure IIP3 are -9 dB and -5.5 dBm respectively. The UWB LNA is consume 34 mW power from 1.5 V supply. Due to high power gain, good linearity, low noise figure and wideband matching of the proposed UWB LNA will

improve performance of the future UWB receiver and it will open new frontier for UWB wireless communication users.

In the day to day life wireless communication applications are increasing. Wireless communication users demand modern mobile terminal should support GSM, UMTS, CDMA, GPS, RFID, Bluetooth, ZigBee, WLAN, LTE, WiMax, etc. different wireless communication standards of 2G, 3G and upcoming 4G technologies. Recently have been observing a paradigm shift in the integrated wireless transceiver design where several narrowband receivers which customized for dedicated applications are replaced by one single receiver which supports different standards operating on different frequencies band. Implementation of the LNA for multi standards receiver is most critical task. Performance of the LNA determines the overall receiver noise figure and sensitivity.

When strong interference signals are received with weak desire signals require highly linear receiver design to avoid blocking. The proposed next design is for highly linear 0.6-5.6 GHz wideband LNA for future multi standards universal receiver. Current reuse NMOS/PMOS inverter structure of amplifier is providing high linearity by cancelling distortion due to complementary characteristics of NMOS and PMOS transistors. Detail analysis of noise figure and input impedance shows resistive feedback inverter LNA topology has tradeoff between NF and matching. The proposed resistive and CD feedback NMOS/PMOS inverter structure design is relax the tradeoff by providing one more degree of freedom to set NF and matching independently. Analysis of CD feedback shows that it is not only relax tradeoff but also reduce noise by cancelling out off phase noise signals. Inductive series and shunt peaking cascode CS amplifier next stage is used with resistive and CD feedback inverter structure first stage to improve overall gain and bandwidth of the design.

Proposed highly linear wideband LNA design is simulated using 0.18 μm RFCMOS MOSFET model. This design achieved very good linearity average IIP3 is + 4 dBm in 0.6-5.6 GHz interested band. Other performance parameters of the LNA, power gain (S_{21}), NF and S_{11} are 20 dB, <4 dB and <-9 dB respectively in 0.6-5.6 GHz wideband. This design is consuming only 13.2 mW power from 1.2 V supply. Results shows the design is highly suitable for implementation of future universal receiver to support GSM, UMTS, CDMA, Bluetooth, ZigBee, RFID, WLAN, LTE, WiMAX, etc. wireless communication

standards. Third high power gain multi standard wideband LNA design is proposed for very high power gain base station universal receiver.

All the LNAs have been designed using TSMC 0.18 μm RFCMOS technology and simulate the designs using Advanced Design System (ADS) RF circuit simulator. These wideband LNA designs are proposed for the next generation wireless receiver implementation. The performance tradeoff among input matching, noise figure, gain and linearity are analyzed in detail and in the research proposed novel circuit techniques for to relax performance tradeoff. The results indicate that the proposed LNAs design will improve performance of the next generation wireless communication.

Acknowledgment

This thesis would have been impossible without support of many people. I would like to express my sincere gratitude to them, though their invaluable support deserves much more than this short note of appreciation. I would like to thanks Almighty the God giving me strength and passion to do research.

I would like to express my sincere appreciation to my supervisor **Dr. Vipul A Shah** for his valuable enthusiastic guidance and encouragement me during every steps of my research. Due to his extensive technical support able complete my research in time. I wholeheartedly give my best wishes to him and his family. I would like to express my sincere gratitude to my co-supervisor **Prof. Durgamadhab Misra** for his valuable technical support.

Also, I would like to express my sincere gratitude to **Dr. Mihir V Shah** and **Dr. Ramji Makwana**. It was great honour to have them as my thesis Doctoral Progress Committee member. Their constructive suggestions made the thesis sound in many aspects.

I would like sincere thanks to **Mr. Bhushan Joshi** for supporting me to learn ADS RF circuit simulation tool. I would like to express my gratitude to **Dr. C. H. Vithalani** and EC department GCET for supporting me whenever needed.

I also acknowledge Honourable Vice Chancellor, Registrar, Controller of Examination, Dean Ph.D. section and all staff members of Ph.D. section of university for their assistance and support.

I would like to express my sincere appreciation to my Ph.D. thesis examiners who have speared his valuable time to evaluate thesis.

Finally, I give the greatest respect and love to my parents, my parents in law, my wife and my son **Manas**. I want to express my highest appreciation for their support and cooperation. I would like to say thanks to my wife **Mrs. Miral** for encourage me to do research and her moral support. Thanks to **Almighty the God** for given me patient to complete research.

This thesis is dedicated to all of my good wisher with my love for assisting me to achieve the most important stage in my life. I will never let them down and wish them all the successes in the future.

Table of Contents

List of Abbreviations

ADC	Analog-to-Digital Conversion
ADS	Advanced Design System
AGC	Automatic Gain Control
BPF	Band Pass Filter
BW	Bandwidth
CDMA	Code Division Multiple Access
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
CD	Common Drain
CP	Carrier Phase
CRLNA	Current Reuse Low Noise Amplifier
DA	Distributed Amplifier
DC	Direct Current
DCS	Digital Cellular Service
DSP	Digital Signal Processing
EIRP	Equivalent Isotropic Radiated Power
FB	Feedback
FCC	Federal Communication Commission
FFT	Fast Fourier Transform
FOM	Figure of Merit
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HPF	High Pass Filter
HSPA	High Speed Packet Access
IC	Integrate Circuit
ID	Inductive Degenerate
IEEE	Institute of Electrical and Electronics Engineering
IIP3	Third order Input Interception Point
IMT	International Mobile Telecommunication Advanced
IR	Impulse Radio

ITU	International Telecommunication Union
KCL	Kirchhoff Current Law
KVL	Kirchhoff Voltage Law
LAN	Local Area Network
LC	Local Oscillator
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LTE	Long Term Evolution
MB OFDM	Multi Band Orthogonal Frequency Division Multiple Access
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NF	Noise Figure
NMOS	N Channel Metal Oxide Semiconductor
OFDM	Orthogonal Frequency Division Multiple Access
OIP	Output Intercept Point
PAN	Personal Area Network
PAM	Pulse Amplitude Modulation
PCS	Personal Communication Service
PMOS	P channel Metal Oxide Semiconductor
PPM	Pulse Position Modulation
PVT	Process Voltage Temperature
RADAR	Radio Detection And Ranging
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RFID	Radio Frequency Identification
SNR	Signal-to-Noise Ratio
TSMC	Taiwan Semiconductor manufacturing Company
UMTS	Universal Mobile Telecommunication System
UWB	Ultra Wideband
VGA	Variable Gain Adjustment
VLSI	Very Large Scale Integration
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	WiFi Local Area Network
WPAN	Wideband Personal Area Network

List of Symbols

μm	Micrometer
nm	Nanometer
GHz	Giga Hertz
K	Boltsman constant
T	Temperature
Δf	Bandwidth
g_m	Transconductance
W	Width of Channel
L	Length of Channel
C_{ox}	Oxide Capacitance
Si	Silicon Substrate
Sio2	Silicon Oxide
dB	Decibel
Ω	Ohm
KΩ	Kilo Ohm
pF	Pico Farad
fF	Facto Farad
nH	Nano Henri
MHz	Mega Hertz
V	Volt
mA	Milli Ampere
Q	Quality Factor

List of Figures

List of Tables

CHAPTER 1

Introduction

1.1 Introduction

The computer will become the hub of a vast network of remote data stations and information banks feeding into the machine at a transmission rate of a billion or more bits of information a second.... Eventually, a global communications network handling voice, data and facsimile will instantly link man to machine—or machine to machine—by land, air, underwater, and space circuits.

—David Sarnoff, 1964

The demand of wireless communication applications push VLSI designer to continuous research in wireless transceiver RFICs design. Application of wireless communication is increasing exponentially. Different wireless standards like GSM, CDMA, UMTS, GPS, Wireless LAN (IEEE 802.11a/b/g), Bluetooth, ZigBee, LTE and WiMax are operate in different frequencies and having different modulation schemes. As per wireless communication users demand future smart phone should support all wireless standards with low power dissipation, less cost and compact size. Currently handsets have separate RF frontend and digital base band processing for each wireless standard which not only require larger silicon area but also consume more power. In order to reduce power dissipation, complex interfacing, cost and area requirement of smart phone, future wireless receiver should have single wideband high performance RF frontend to support all wireless communication standards. The LNA designing is most critical task in RF frontend and its performance impact in overall performance of RF receiver.

1.2 Universal Receiver

All wireless standards receiver should integrate in single chip with hardware sharing and reusing as per future demand. The receiver which supports all wireless communication standards is known as universal receiver.

Ideal universal receiver architecture proposed by mitiola [1] is shown in Fig. 1.1. Implementation of ideal universal receiver for RF is still not reality because of it puts very tough design requirements of Analog to Digital Conversion (ADC) to process low amplitude RF signal. Designing of ADC for RF universal receiver is impossible task using current technology. Practical universal receiver architecture is incorporating Low Noise Amplifier (LNA) and mixer as shown in Fig. 1.2. Mixer is relaxed the speed performance requirement of the ADC by down conversion of frequency. An LNA relaxes dynamic range, noise and linearity performance requirements of the ADC, hence Low Noise Amplifier is essential to implement any RF receiver.

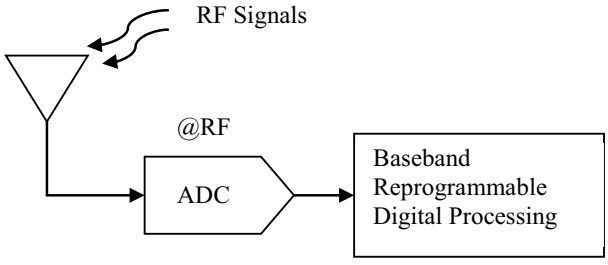

FIGURE 1.1: Ideal universal radio architecture.

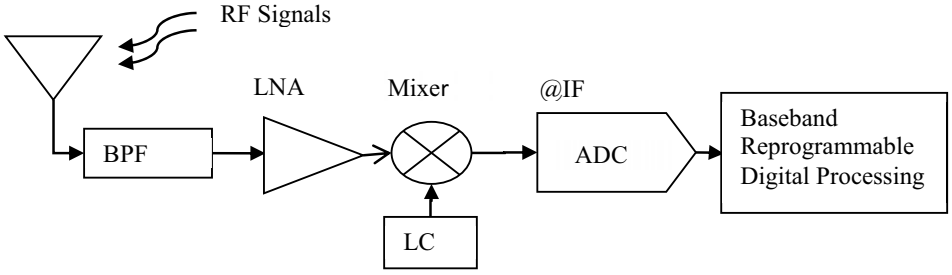

FIGURE 1.2: Practical universal radio architecture.

Designing of the LNA for universal receiver is still a challenging task. At present multi standards receiver designs are dedicated to optimized for specific wireless standard and obtain best performance but at higher cost and more power consumption. The universal

receiver has key advantages, such as reconfigurable, low complexity, low power dissipation and no image frequency as compare to super heterodyne receiver architecture.

Digital RF is another architecture in addition to universal receiver used for RF receiver [2]. In digital RF receiver architecture all tradition block such a mixer and filter are replaced by its digital counterpart. The main problem in implementation of digital RF receiver is its high speed sampling, which introduce more noise. Signal to Noise Ratio (SNR) of the input signals in the digital RF receiver need to increase for noise reduction. There for, the Low Noise Amplifier becomes essential component for universal and digital RF receiver. Still there is no receiver architecture for RF wireless communication that can eliminate the need of LNA.

Multi wireless standards receiver requires high power gain, low noise figure, high linearity and wideband input matching LNA. Overall receiver sensitivity depends on gain and Noise Figure (NF) performance of LNA, linearity of the system depends on transfer function and reverse isolation of the LNA. The designing of wideband LNA for universal receiver pose many challenges and it is emphasized in the thesis.

1.3 Introduction of UWB System

Federal Communications Commission (FCC) has approved ultra wideband (UWB) 3.1-10.6 GHz frequency band for commercial use in 2002 with restriction to transmit information using low power. Extremely wide bandwidth of UWB system provides high transmission channel capacity and less multi path fading. So it opens new frontier for wireless communication users. The UWB system is widely used in high data rate wireless communication, image penetration and high accuracy locating applications.

Despite all the favorable features of the UWB systems, serious challenges exist for the realization of 3.1-10.6 GHz wideband high power gain Low Noise Amplifier (LNA) for UWB RF frontend. FCC's limit transmitter power and due to addition path loss receiver receive low power signals. Process low power received signals UWB receiver requires high power gain and low noise figure wideband matching LNA. One of the objectives of this research work is analyzed and design high power gain 3.1-10.6 GHz UWB LNA for UWB receiver.

1.4 The CMOS Technology

Before 1980s discrete components, such as transistors, resistors, capacitors and inductors were widely used to design RF receive circuits. The discrete design of RF receiver was bulky, expensive and poor performance. The advancement in VLSI technology has replaced discrete components based implementation of wireless receiver using RFIC. The Complementary Metal Oxide Semiconductor (CMOS) is advanced enough to implement any wireless communication applications system. The CMOS technology has low fabrication cost and high level of integration, so it is more attractive solution of RFIC. The realization of passive components like resistors, capacitors and inductors using CMOS will increase speed, reduce size and cost of RF receiver. 0.18μm RFCMOS technology is the targeted process for the work due to its low fabrication cost, good technology performance, good Ft (unity gain cutoff frequency) and good linearity. The unity gain cut off frequency of 0.18 μm RFCMOS technology is good enough to provide high gain up to 15 GHz frequency.

1.5 Definition of the Problem

After the two decade of research in RFIC circuit designing, it is still challenging due to three factor (i) RFIC design require multidiscipline knowledge of the IC designing, microwave theory, transceiver architectures, communication theory, wireless standards, Random signals, CAD tools, Multiple access, and Signal Propagation. (ii) RF circuit design deal with trade-offs of Gain, Power consumption, Noise, Linearity and Bandwidth (iii) the demand of high performance, low cost, low power and greater functionalities. These three challenging factors of RFIC design push VLSI researcher to do research in implement of RFIC.

Wireless communication applications are increased rapidly which leads to challenge wireless RF circuit's designer to design RFIC for next generation wireless communication receiver. Objective of this research work is to analyze, design and implementation of two narrowband LNAs for Bluetooth and Global Positioning System (GPS) receiver, three wideband LNAs for future multi standards universal and UWB receiver.

- Due to FCC restriction on power transmission in use of UWB for commercial wireless applications require low noise high power gain receiver to amplify and process received weak signals. For this two approaches can be used to implement LNA for UWB receiver either multiple LNA chain for each band of UWB or

- single 3.1-10.6GHz wideband LNA. The second approach, 3.1-10.6GHz wideband LNA not only reduce silicon area requirement but also reduce power consumption. To improve performance of UWB system requires high power gain, low noise figure and wideband matching 3.1-10.6GHz wideband LNA.

- To support existing 2G and 3G GSM, UMTS, CDMA, Bluetooth, ZigBee, GPS, WLAN with future 4G LTE and WiMAX wireless communication standards requires high performance RF Frontend receiver. The performance of LNA decides overall performance of receiver. Next generation multi standard receiver will require 0.6-5.6GHz wideband, High gain, Low noise Figure, good linearity and wideband input matching LNA to support future wireless standards.

1.6 Objective and Scope of the Work

The design of LNA for future universal receiver is still a challenging task. The next generation multi standards multi-mode wireless communication applications require high power gain, highly linear wideband RF front end. The implementation of multi-mode multi standard receiver using multi transceiver which not only requires larger silicon area but also consumes more power and it is not suitable for battery operated device. Universal radio receiver architecture has wideband transceiver, which support multi standards wireless communication applications and reduce silicon area and power consumption. Objective of this research work is to design wideband LNAs for next generation universal and UWB system receiver.

1.7 Original Contribution by the Thesis

Original contribution of the thesis is propose analyze, design of two narrowband LNAs for Bluetooth and GPS receiver and three wideband LNAs for multi standards next generation and UWB system receiver. All the LNAs are design using 0.18 µm RFCMOS and simulate the designs using Advance Design System RF simulator tool.

- The thesis contributes detailed analysis of input matching, gain and noise figure of inductive degenerate common source (IDCS) topology of Low Noise Amplifier (LNA). The Narrowband LNAs are designed using IDCS topology for Bluetooth

and GPS receiver. Portable Bluetooth receiver LNA is designed using current reuse topology to reduce power consumption, which will improve battery lifetime.

- In this research work, proposed high power gain 3.1-10.6 GHz UWB LNA for commercial applications. The first stage of proposed design is inductive source Common Gate (CG) for wideband matching. Input impedance and noise figure of CG are analyzed in detail and optimized the design for low noise figure. CG has low power gain which can be improved by using two cascade CS stages. To reduce noise in this design inductive load is used instead of resistive in each stage. The inductive load not only reduces noise but also increases gain by forming parallel tune circuit with next stage input capacitor. The bandwidth of this LNA is increased by resonating each output parallel tune circuit at different frequencies. The results shows proposed LNA design is highly suitable to increase performance of UWB receiver.

- The proposed 0.6-5.6GHz wideband LNA design has highly linear and high power gain to support multi standards future universal receiver. To support LTE and WiMAX 4G standards with existing GSM, CDMA, UMTS, Bluetooth, ZigBee and WLAN standards require 0.6-5.6 GHz wideband matching, high linearity, high gain and low noise figure receiver. Distortion cancellation analysis of NMOS/PMOS inverter structure carried outs, resulted as inverter structure provides good linearity. Analyzed input capacitance and efficiency factor of inverter structure amplifier and proposed solution to cancel the effect of input capacitance to improve gain at higher frequency. There is tradeoff between low noise figure and wideband matching in selection of feedback resistance value of resistive feedback inverter LNA. In the research propose, the design of LNA to relax tradeoff between low noise figure and wideband matching. The novel highly linear LNA design is based on common drain and resistive feedback inverter structure with series and shunt peaking inductors CS next stage for future mobile terminal.

The research work published in peer review international journals and IEEE internal conferences.

1.8 Thesis Organization

Thesis is organized in seven different chapters including this introduction chapter 1.In Chapter 2, introduce the fundamental concepts of LNA. The S parameter and it use in two port network analysis is discussed. The different performance parameters of LNA relevant to receiver are introduced, such as impedance matching, noise figure, Power gain, harmonic distortion and stability.

In chapter 3, a wideband LNA state of art has been discussed. Different wideband topologies are analyzed in details with pros and cons. Each wideband topology performance parameters like input impedance, noise figure are analyzed in detail and tradeoff among them are discussed.

Chapter 4 covers the design steps of narrowband LNA using inductive source degenerate topology. The Bluetooth receiver narrowband LNAs are designed using inductive degenerate common source as well as current reuse topology. The Global Positioning System (GPS) requires high sensitive receiver to receive weak GPS signals. The chapter also covers design and simulation of narrowband LNAs for GPS receiver using IDCS and current reuse topology. The end of the chapter compares the proposed LNAs performance with published work.

Chapter 5 covers detailed analysis and designing of high power gain UWB LNA for UWB wireless applications. Input impedance and noise figure of Common Gate stage of the proposed UWB LNA design is analyzed. The LNA design is optimized for low noise figure. The proposed LNA is design using 0.18μm RFCMOS technology and the design simulated using Advanced Design System RF simulation tool. The simulation results show the design having wideband input matching, high power gain and low noise figure compare to published work.

Chapter 6 covers the detailed analysis of distortion cancellation of NMOS/PMOS inverter structure. The chapter covers analysis and design of gate inductor based LNA to improve gain and input matching at higher frequency. The complete analysis of resistive feedback NMOS/PMOS structure LNA is carried out in this chapter. The chapter covers analysis, design and simulation of Common Drain (CD) active and resistive feedback inverter structure. Performance parameters of CD active feedback inverter LNA design is analyzed. At the end of the chapter proposed, design and simulate highly linear multiple negative

feedback inverter structure with inductive series and shunt peaking CS LNA topology for the next generation universal receiver to support existing 2G, 3G along with coming 4G wireless standards. Also, in the chapter covers design and simulation of high power gain LNA for base station universal receiver. The chapter ends with comparison of achieved performance of proposed LNAs with published work.

In last chapter 7 Concludes the work with major contributions and also discusses future scope to extend the work.

CHAPTER 2

LNA Fundamentals

2.1 S Parameters

At RF frequency S parameter is widely used to describe two port networks instead of Z, Y, ABCD and H parameters. The S parameters are defined in terms of incident and reflected waves. As shown in Fig. 2.1 a_1 and b_1 are incident and reflected waves of port1 respectively and a_2 and b_2 are incident and reflected waves of port2 respectively.

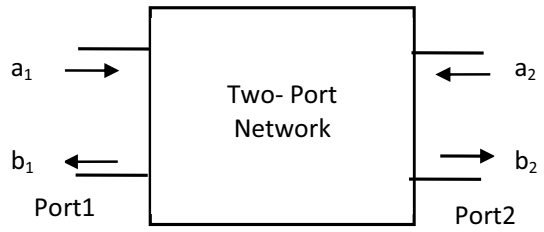

FIGURE 2.1: Two port network.

The b_1 and b_2 are dependent on the a_1 and a_2 and relationship between the incidents and reflected waves are described using (2.1) and (2.2).

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.2}$$

Equation (2.3) shows matrix representation of (2.1) and (2.2).

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.3}$$

The S parameters are easily understood by (2.1) and (2.2). The S_{11} is defined as

$$S_{11} = \frac{b_1}{a_1} | \; at \; a_2 = 0 \tag{2.4}$$

S_{11} shows how much of a_1 is reflected back to b_1. S_{11} shows measure of input matching for maximum power transfer. If reflected power b_1 is 0, means all input power is transferred. The value of S_{11} is 0 or in logarithmic value -∞ which shows perfect matching. The practical value of S_{11} should be as low as possible for maximum power transfer and below -10 dB is preferable. The S_{12} is defined as

$$S_{12} = \frac{b_1}{a_2} | \; at \; a_1 = 0 \tag{2.5}$$

Value of S_{12} shows how much power is transferred from port2 to port1. S_{12} measure how good is the isolation between port1 and port2, and its value should be as low as possible for better isolation from port2 to port1. The S_{21} is defined as

$$S_{21} = \frac{b_2}{a_1} | \; at \; a_2 = 0 \tag{2.6}$$

S_{21} is ratio between output power at port2 and input power at port1. It shows power gain of two port network. Similarly S_{22} is defined as

$$S_{22} = \frac{b_2}{a_2} | \; at \; a_1 = 0 \tag{2.7}$$

S_{22} measures output port matching. Value of S_{22} should be as low as possible for better port2 matching with load so that it can transfer maximum power to load.

A good amplifier should have S_{11}, S_{22} and S_{12} low and S_{21} high. S_{11} is used to measure the input match and S_{21} is used to measure power gain of the LNA.

The stability of the two port network is analyzed using S parameters. The necessary condition for stability is expressed in terms of S parameters as (2.8).

$$K = \frac{1-|S_{22}|^2-|S_{11}|^2+|\Delta_s|^2}{2|S_{12}S_{21}|} > 1 \tag{2.8}$$

Where, $\Delta_s = S_{11}S_{22} - S_{12}S_{21}$. Two port network is stable if it satisfy condition given in (2.9)

$$||\Delta_s|^2 - L| + L > 1 \tag{2.9}$$

Where, $L = |S_{12}S_{21}| + \frac{|S_{11}|^2+|S_{22}|^2}{2}$

2.2 Low Noise Amplifier (LNA) Performance Parameters

Major performance parameters of the LNA are:

- Noise Figure (NF)
- Power Gain (S_{21}) and Input matching (S_{11})
- Linearity (IIP3)
- Power consumption
- Stability

2.2.1 Noise Performance

The Noise performance of two port network is measured using Noise Factor (F). The noise factor is defined as the ratio of the total output noise power to the output noise due to input source. If the Noise Factor is expressed in decibels it is called the Noise Figure (NF).

$$\mathrm{SNR} = \frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}}} \tag{2.10}$$

$$\mathrm{F} = \frac{{}^{\mathrm{P_{si}}}/_{\mathrm{P_{ni}}}}{{}^{\mathrm{P_{so}}}/_{\mathrm{P_{no}}}} \tag{2.11}$$

$$\mathrm{NF} = 10\log(\mathrm{F}) \tag{2.12}$$

Where, P_{si} is input signal power, P_{ni} is the input noise power, P_{so} is the output signal power and P_{no} is the output noise power. Overall noise figure of multistage amplifier receiver is express as

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \ldots A_{p(m-1)}} \tag{2.13}$$

Equation 2.13 is also known as Friis formula which is named after the Danish-American electrical engineer Harald T. Friis. The first amplifier stage of receiver contribute major portion of overall noise. The first amplifier stage of receiver is known as Low Noise Amplifier (LNA). This is the rationale behind why the first stage of amplifier has to a low noise figure as possible.

NOISE DEFINITION: Noise arises in electronic circuits as a random variable and is non-deterministic. Noise generated in circuit is due to nature of the materials or by external interferences. Signal degrades due to noise. So it is needed to carefully analyze and develop method to minimized effect of noise on signals. In following section, the main noise sources present in circuit are described. [3] [4].

THERMAL NOISE: Thermal noise in circuits is due to the random motion of electrons. Thermal noise signal power is expressed as (2.14)

$$P = kT\Delta f \tag{2.14}$$

Where k is the Boltzmann's constant, T is the temperature in Kelvin, and Δf is the bandwidth in Hz of the system. Thermal noise voltage generated in resistor is modeled as (2.15).

$$\overline{V_{th}^2} = 4kTR\Delta f \tag{2.15}$$

Where, R is resistance value in ohm. Similarly thermal noise current produce in resistor is expressed using (2.16).

$$\overline{I_{th}^2} = \frac{4kT\Delta f}{R} \tag{2.16}$$

MOSFET also exhibit thermal noise due to the carrier motion in the channel. This noise is modeled by putting current source in parallel MOSFET with conducting channel as shown in Fig. 2.2. This noise current modeled when device operate in triode mode as (2.17). [5]

$$\overline{I_n^2} = 4kT\gamma g_{d0}\Delta f \tag{2.17}$$

Where, γ is the excess noise parameter and g_{d0} is the drain to source conductance for V_{DS} = 0. When MOSFET operate in saturation mode channel thermal noise current modeled as it shown in (2.18). [6]

$$\overline{I_n^2} = 4kT\gamma g_m\Delta f \tag{2.18}$$

Where, γ= 2/3 [7] for long channel device, For short-channel and submicron MOSFETS, γ has higher values, in a range between 1 and 3 [8].

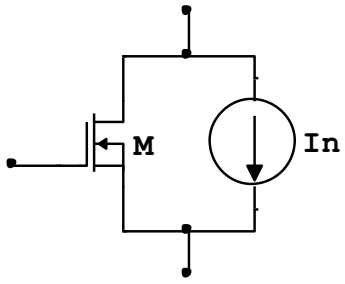

FIGURE 2.2: MOSFET channel thermal noise representation.

DISTRIBUTED GATE RESISTANCE NOISE: Another source of noise in MOSFET is thermal noise generated by distributed gate resistance. This gate resistance is dependent on the MOSFET geometry. The gate resistance for a single polysilicon gate finger, connected on both sides is expressed as (2.19) [9].

$$R_G = \frac{1}{12}\rho_{sh}\frac{W}{L} + \frac{\rho_{con}}{WL} \tag{2.19}$$

Where, ρ_{sh} is silicide sheet resistance, W and L is the width and length of the MOSFET channel and ρ_{con} is silicide to polysilicon contact resistance.

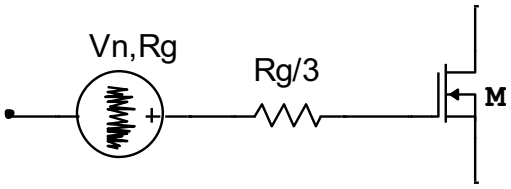

FIGURE 2.3: Equivalent noise model for gate resistance.

In Fig. 2.3 shows equivalent noise model of gate resistor where $R_G/3$ is equivalent gate resistance and Vn,Rg is equivalent gate noise voltage [4] [10].

Effective silicide sheet resistance can be reduce by using multi fingers gate design [9], [11] and it decrease gate resistance thermal noise. If value of power spectral density of this noise is very less than channel thermal noise, then it can be neglected.

$$4kT\frac{R_G}{3} \ll \frac{4kT\gamma}{g_m} \tag{2.20}$$

FLICKER NOISE: The flicker noise in MOSFET is due to a physical phenomenon, and it is unpredictable. It is related with the interface between the silicon substrate (Si) and gate oxide (Sio2). The flicker noise is due to random fluctuation of carriers in the channel, caused by trapping and release of carriers in the Si and SiO2 interface. Flicker noise is proportional to 1/

f, so it is neglected at higher frequencies. It is model by a flicker noise voltage source in series with the gate. The flicker noise is modeled using (2.21).

$$\overline{V_{nf}^2} = \frac{k_f}{C_{ox}WLf} \tag{2.21}$$

Where, k_f is a process dependent constant, and C_{ox}, W, and L are the gate oxide capacitance per unit area, width, and length of the MOSFET respectively. For p-channel devices k_f is lower than for n-channel devices, and thus PMOS transistors have less flicker noise.

SHOT NOISE: Shot noise is caused by fluctuation of the current that crosses a pn junction potential barrier. The diffusion of charge carriers is random and cause different speed of carriers. The shot noise defined as (2.22).

$$\overline{I_{ns}^2} = 2qI_{DC} \tag{2.22}$$

Shot noise is originating the fluctuation of current around an average value. Where, q is the electron charge and I_{DC} is the DC current. Shot noise is more significant in bipolar junction transistors compared to MOSFET because both emitter and collector currents are sources of shot noise. In MOSFETs, the DC gate leakage current contributes shot noise and it is usually very small and in most cases it can be neglected.

The sensitivity of a receiver is defined based on what minimum signal power can be processed by receiver. Receiver sensitivity is determined from minimum signal to noise ratio (SNR), Noise figure and noise power.

$$P_{sens} = SNR_{Rxmin} + P_{n,s} + NF_{Rx} \tag{2.23}$$

where, P_{sens}, SNR_{Rxmin}, $P_{n,s}$ and NF_{Rx} are receiver power sensitivity in terms of dBm, minimum SNR in dB, source noise power in dBm and the noise figure in dB of the receiver respectively. If sensitivity, transmitted power and path loss knows maximum distance of communication take place can be find. Therefore minimum noise figure of receiver is desired to improve sensitivity of receiver. The LNA first stage of receiver should have low noise figure in order to reduce overall noise figure and better sensitivity of receiver. Most of Communication standards required SNR, sensitivity and NF are specified in Table 2.1. NF below 4dB of LNA is expected in most of communication standards.

TABLE 2.1: Sensitivity, SNR and Noise Figure specification of different standards receiver.

	GSM	WCDMA	Bluetooth	RFID	WLAN	LTE	WiMAX
P_{sens} (dBm)	-102	-117	-70	-70	-65	-102	-65
SNR (dB)	9	5.2	21	11.6	28	8	24
NF (dB)	9	9	23	39	7.5	9	7

2.2.2 Power Gain and Impedance Matching

LNA is the first amplifier stage in receiver to amplify weak signals incoming from antenna. For maximum power transfer from output of antenna to input of LNA require input impedance of LNA match to the output impedance of antenna. If impedance does not match, signal is reflected back and cause noise. To maximize power transfer input impedance matching is very important parameter in LNA design. S_{11} of two port network S parameter indicate ratio between reflected signal powers to the input signal power at port 1. S_{11} is measure in dB and below -10 dB of S_{11} is desired. -10dB of S_{11} mean 10% of total input power reflected back. Similarly, output impedance of LNA should match with next stage input impedance for maximized transfer of amplified output power of LNA to next stage input. Output impedance matching is measured by S_{22} of S parameter. Other design performance parameter is Power gain (S_{21}), it should be as high as possible to increase strength of weak received signals.

2.2.3 Linearity

In the LNA design linearity is another importance parameter to be considered when receiving weak input signals with strong interfering signals. Strong interference signals is produce cross modulation and blocking undesired inter modulation distortion in poor linear system.

DEFINITION OF NONLINEARITY: For memoryless linear system input output relationship is defined as (2.24)

$$y(t) = \alpha x(t) \tag{2.24}$$

Where α is a function of time if system is time variant or a constant for time invariant system. For memoryless nonlinear system input/output relationship is define as (2.25) [12].

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots, \tag{2.25}$$

HARMONIC DISTORTION NONLINEARITY: If $x(t) = Acos(wt)$ sinusoidal is applied to nonlinear system, then it produces output as

$$y(t) = \alpha_1 A\, cos\, \omega t + \alpha_2 A^2 cos^2 \omega t + \alpha_3 A^3 cos^3 \omega t \quad (2.26)$$

$$= \alpha_1 A\, cos\, \omega t + \frac{\alpha_2 A^2}{2}(1 + cos\, 2\omega t) + \frac{\alpha_3 A^3}{4}(3cos\, \omega t + cos\, 3\omega t) \quad (2.27)$$

$$= \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})cos\, \omega t + \frac{\alpha_2 A^2}{2}(cos\, 2\omega t) + \frac{\alpha_3 A^3}{4}(cos\, 3\omega t) \quad (2.28)$$

In (2.28) the first term on right-hand side is a dc quantity arising from second-order nonlinearity, the second term is fundamental component with multiplication gain factor, the third term is second harmonic distortion and the fourth term is the third harmonics distortion. Harmonic distortion is not a major nonlinearity because suppose amplifier operating at 2.4 GHz produce second harmonic at 4.8 GHz which is out off band of filter [12].

GAIN COMPRESSION NONLINEARITY: Formulation of harmonics shows gain experienced by $Acos(wt)$is equal to $(\alpha_1 + \frac{3\alpha_3 A^2}{4})$ and hence varies noticeably as A becomes larger. If α1α3<0 which make decreasing gain as an A increase. This effect can be measured with 1dB Gain Compression point, which can be define as the input power level of signal which causes the gain to drop by 1dB from its interpolated extended value as shown in figure 2.4. If plotted in logarithmic scale as a function of input power at a 1dB compression point output power fall 1dB from its ideal value [12].

The 1 dB compression point can be calculated by equating compressed gain to 1dB less than the ideal gain

$$20log(\alpha_1 + \frac{3\alpha_3 A^2}{4}) = 20\log(\alpha_1) - 1dB \quad (2.29)$$

Gain A at this point is called $A_{in,\,1dB}$ and it can be found from solving (2.29)

$$A_{in,1dB} = \sqrt{0.145 \left|\frac{\alpha_1}{\alpha_3}\right|} \quad (2.30)$$

The 1 dB compression means 10% reduction in gain and it's widely used to characterize RF systems.

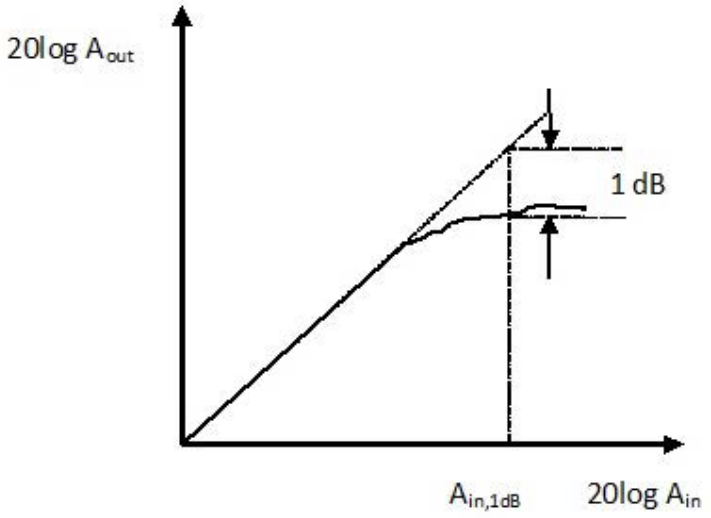

FIGURE 2.4: 1dB compression point.

Another adverse effect from compression occurs if strong interfering signal goes along with the received signal. In the time domain, the weak desired signal is superimposed on the strong interfering signal. Due to that, gain of receiver is reduced by the large excursion produced by the interferer even though the desired signal itself is small and is called as "desensitization". This phenomenon lowers the signal to noise ratio (SNR) at the output and proves critical even if the signal contains no amplitude information [12].

For the qualitatively measure desensitization, let us assume $A_1 \cos(w_1 t)$ is desire signal and $A_2 \cos(w_2 t)$ is interferer signal so input to amplifier is $x(t) = A_1 \cos(w_1 t) + A_2 \cos(w_2 t)$ Nonlinear system output appear as

$$y(t) = \left(\alpha_1 + \frac{3}{4}\alpha_3 A_1^2 + \frac{3}{2}\alpha_3 A_2^2\right) A_1 cos\ \omega_1 t + \cdots \tag{2.31}$$

For $A_1 \ll A_2$, this reduce to

$$y(t) = \left(\alpha_1 + \frac{3}{2}\alpha_3 A_2^2\right) A_1 cos\ \omega_1 t + \cdots \tag{2.32}$$

Thus, the gain experienced by the desired signal is equal to $\left(\alpha_1 + \frac{3}{2}\alpha_3 A_2^2\right)$, a decreasing function of A_2 if $\alpha_1 \alpha_3 < 0$. Larger value of A_2 make gain drop to zero, this condition is called signal blocking. In RF design the term blocking signal or blocker refers to interferers that desensitize a circuit even if they do not reduce the gain to zero [12].

CROSS MODULATION NONLINEARITY: When weak desire signal with large interfering signal pass through poor linear system, then it transfer modulation in desire signal from interfere this phenomena is called cross modulation. To understand cross modulation effect, let us take modulated interferer signal $A_2(1 + mcos\omega_m t)cos\omega_2 t$ with desire signal $A_2(cos\omega_1 t)$ passing through a nonlinear system produce output

$$y(t) = \left[\alpha_1 + \frac{3}{2}\alpha_3 A_2^2(1 + \frac{m^2}{2} + \frac{m^2}{2}cos2\omega_m t + 2mcos\omega_m t)\right] A_1 cos\omega_1 t + \cdots \quad (2.33)$$

The (2.33) says that desired signal suffer from amplitude modulation at ω_m and $2\omega_m$ frequency. Cross modulation nonlinearity effect is graphically illustrate in Fig. 2.5.

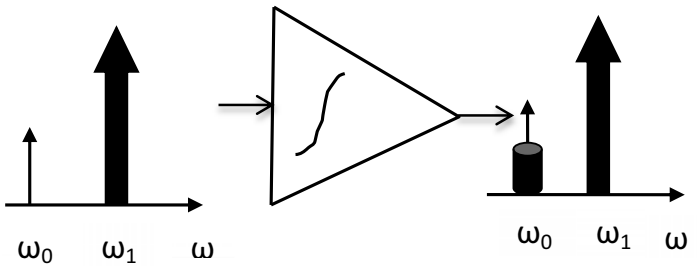

FIGURE 2.5: Cross modulation nonlinearity effect.

All above nonlinearity effect consider only single signal. Another nonlinearity effect occurs if two interferes accompany the desired signal. If two interferers of different frequency ω_1 and ω_2 are applied to a nonlinear system then produce output generally contain components that are not the harmonics of ω_1 and ω_2 frequencies called intermodulation. To understand intermodulation let take $x(t) = A_1 cos\omega_1 t + A_2 cos\omega_2 t$ combination interferers signals as input to any nonlinear system. Output is

$$y(t) = \alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2 t) + \alpha_2(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^2 + \alpha_3(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^3 \quad (2.34)$$

Expanding above equation and discarding dc, harmonics, and components at $\omega_1 \pm \omega_2$ terms following intermodulation products are obtained:

$$\omega = 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 - \omega_2)t \quad (2.35)$$

$$\omega = 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_1 A_2^2}{4} cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_1 A_2^2}{4} cos(2\omega_2 - \omega_1)t \quad (2.36)$$

And fundamental components:

$\omega = \omega_1, \omega_2$:

$$\left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right) cos\omega_1 t + \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2\right) cos\omega_2 t \qquad (2.37)$$

Small desired signal at ω_0 along with two large interferers at ω_1 and ω_2 received by an antenna and providing this to a low noise amplifier. Let us assume that the interferer frequencies happen to satisfy $2\omega_1 - \omega_2 = \omega_0$. Intermodulation product at $2\omega_1 - \omega_2$ falls onto the desired channel and corrupt the signal [13]. Third order intermodulation nonlinearity effect on desire signal due to two strong modulated interference signals, graphically shown in Fig. 2.6.

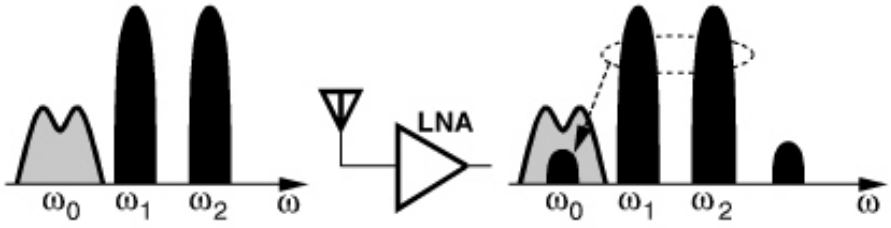

FIGURE 2.6: Third order intermodulation nonlinearity effect [12].

Third order hamonics amplitude increase with A^3 . when power of fundmental and third order harmonic components are equal corrosponding input power called input intermodulation product (IIP3) and at that point output power called output intermodulation product (OIP3). IIP3 and OIP3 can be found plotting input power versus output power as shown in Fig. 2.7.

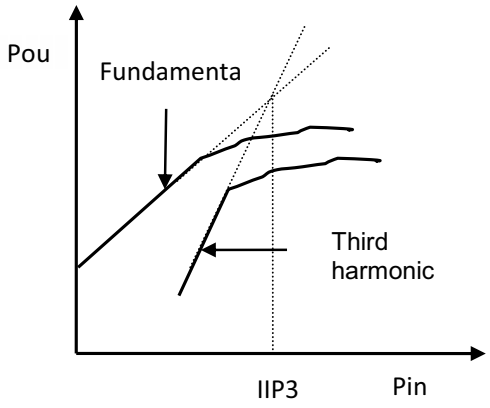

FIGURE 2.7: Intermodulation product

By equating fundamental and intermodulation amplitudes we can find IIP3:

$$|\alpha_1 A_{IIP3}| = \left|\frac{3}{4}\alpha_3 A_{IIP3}^3\right| \tag{2.38}$$

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.39}$$

From above equation relationship between AIIP3 and A1dB is

$$\frac{A_{IIP3}}{A_{1dB}} = \sqrt{\frac{4}{0.435}} \approx 9.6dB \tag{2.40}$$

1 dB compression point (P1dB) and third order intercept (IIP3) are used to measure linearity of system. IP3 shows that power level at which the third order intermodulation product is equal to the first order output power. Third orders input intercept point (IIP3) and output intercept point (OIP3) are the input power and output power respectively at IP3. A_{1dB} defines as input power level when output power drops 1 dB from its theoretical linear value. A_{IIP3} and A_{1dB} have an approximation relation A_{IIP3}= A_{1dB} +10 dBm [12]. Typical IIP3 value require for different standards receiver are given in Table 2.2.

TABLE 2.2: IIP3 requirements in different standards receiver.

	GSM	WCDMA	Bluetooth	RFID	WLAN	LTE	WiMAX
IIP3 (dBm)	-18	-4	-15	-20	-20	-7	-8

2.2.4 Power Consumption

Power consumption is very important design parameter for battery operated devices. Low power dissipation design not only increases battery life but also decrease cost of cooling system and allow to increased complexity of chip to incorporate more functionality.

2.2.5 Stability

In the high power gain MOSFET based amplifier design care have be taken that the design remain stable in all input and output loading condition. A widely used metric for study of the stability characteristics based on S parameters involves the use of the stability factor K, given by the expression (2.41).

$$K = \frac{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad (2.41)$$

Where, $\Delta = S_{11}S_{22} - S_{21}S_{12}$, determinant of S parameter matrix. Value of K greater than unity and Δ less than unity make system unconditionally stable.

From the expression for K, amplifiers with high power gain (S_{21}) require the feedback parameter S_{12} to be small. The cascode amplifier circuit improves overall stability by reducing the gain at the output of the driver transistor, which makes the device more unilateral.

As we can see, the design of an LNA is a multi-dimensional optimization problem. There are lots of trade-offs involved because the optimization of each individual specification does not arrive at the same sizing or biasing solution. This emphasize the designer consider the best combination of performance specifications for the intended application of the LNA.

CHAPTER 3

Literature Review

3.1 Wideband LNA Implementation Approaches

Multi standards LNA can be implement using three different approach (a) Using separate narrowband LNAs for each communication standard, which is easy to design and it has achieve good performance but due to multiple LNAs consume high power and require large silicon area [14, 15, 16, 17, 18, 19, 20], (b) Using multiband/band switching LNA. Multiband allows power saving compare to narrow band LNAs but occupies large area due to implementation of higher value of tuning inductors [21, 22, 23, 24, 25, 26], (c) Third approach is using single wideband LNA to support all standards simultaneously. Wideband LNA has low cost and requires small area compared to first and second approach but demerit of this is low power gain [27, 28, 29, 30, 31, 32, 33, 34]. Wideband LNA is good solution to accommodate multiple standards [34]. Wideband LNA provides flat gain, input impedance matching, NF and IIP3 in their entire bandwidth.

Several topologies are used in literature for wideband input matching are (a) Resistive termination common source, (b) Common gate, (c) Feedback, (d) CS with wideband input filter and (e) Distributed as shown in Fig. 3.1 and Fig. 3.2.

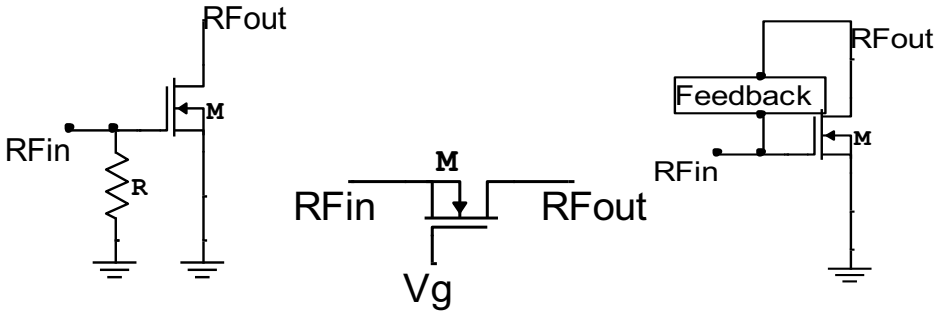

FIGURE 3.1: a) Resistive termination, b) common gate, c) feedback LNA topology.

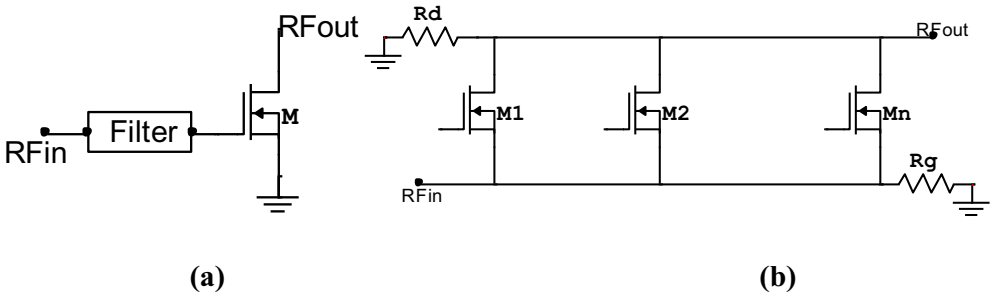

FIGURE 3.2: a) Filter and b) Distributed LNA topology.

3.2 Common Source with Resistive Termination LNA Topology

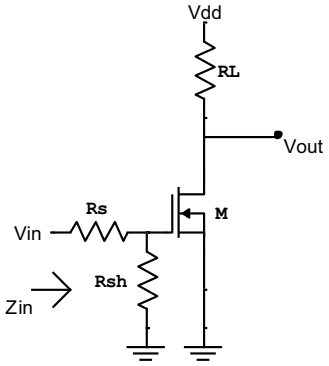

FIGURE 3.3: Common Source (CS) with resistive termination topology.

One of the approach to achieve wideband input impedance matching is adding shunt resistor at input of the CS LNA [3] as shown in Fig. 3.3.

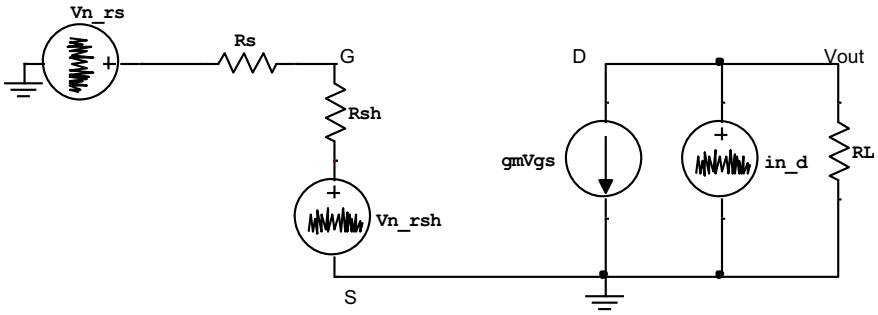

FIGURE 3.4: AC equivalent circuit with noise sources of resistive termination CS.

Voltage gain of resistive termination is expressed as

$$A = -g_m R_L \left(\frac{R_{sh}}{R_s + R_{sh}}\right) \tag{3.1}$$

For $R_{sh} = R_s$ voltage gain is simplified as

$$A = -g_m \frac{R_L}{2} \tag{3.2}$$

As shown in (3.2) Gain of the resistive termination at input matching is half compared to Common source gain $-g_mR_L$. Noise figure is defined as

$$F = \frac{Total\ output\ noise\ power}{Output\ noise\ due\ to\ input\ source}$$

Noise generated by source resistor, termination resistor and MOSFET channel noise are modeled as (3.3), (3.4) and (3.5).

$$\overline{V_{n,Rs}^2} = 4kTR_s\Delta f \tag{3.3}$$

$$\overline{V_{n,Rsh}^2} = 4kTR_{sh}\Delta f \tag{3.4}$$

$$\overline{I_d^2} = 4kT\gamma g_m\Delta f \tag{3.5}$$

Total noise generated at output can be calculated by using superposition, considering one at a time. Output noise due to source resistor express as (3.6)

$$\overline{V_{on,Rs}^2} = \overline{V_{n,Rs}^2} \times A^2 = \overline{V_{n,Rs}^2} \times g_m^2R_L^2 \times \left(\frac{R_{sh}}{R_s+R_{sh}}\right)^2 \tag{3.6}$$

Output noise due to shunt resistor is

$$\overline{V_{on,Rsh}^2} = \overline{V_{n,Rsh}^2} \times A^2 = \overline{V_{n,Rsh}^2} \times g_m^2R_L^2 \times \left(\frac{R_{sh}}{R_s+R_{sh}}\right)^2 \tag{3.7}$$

Output noise due to MOSFET drain current noise is

$$\overline{V_{on,d}^2} = \overline{I_{n,d}^2} \times R_L^2 \tag{3.8}$$

Total noise figure of this topology express using superposition theorem is analyzed as

$$NF = \frac{\overline{V_{on,Rs}^2}+\overline{V_{on,Rsh}^2}+\overline{V_{on,d}^2}}{\overline{V_{on,Rs}^2}} = 1 + \frac{\overline{V_{on,Rsh}^2}+\overline{V_{on,d}^2}}{\overline{V_{on,Rs}^2}} \tag{3.9}$$

At impedance match $R_s = R_{sh}$ so, NF simplify as

$$NF = 1 + 1 + \frac{R_L^2\gamma g_m}{R_s \times \frac{g_m^2R_s^2 \times R_L^2}{4R_s^2}} = 2 + \frac{R_L^2\gamma g_m}{R_s \times \frac{g_m^2 \times R_L^2}{4}} \tag{3.10}$$

$$NF = 2 + \frac{4\gamma}{g_m R_s} \tag{3.11}$$

Where, γ is a noise parameter and $R_s = R_{sh}$ is shunt resistor value. Limitations of this topology are:

- Poor noise figure
- Input signal attenuated by voltage divider and it reduce gain
- R_{sh} adds extra thermal noise
- At higher frequency, to match extra shunt inductor requires to tune out input capacitance $c_{gs.}$

3.3 Common Gate Topology

The Common Gate (CG) amplifier has inherent wideband input matching characteristics [22]. Input impedance of common gate is expressed as (3.12).

$$Z_{in} = \frac{1}{g_m} \tag{3.12}$$

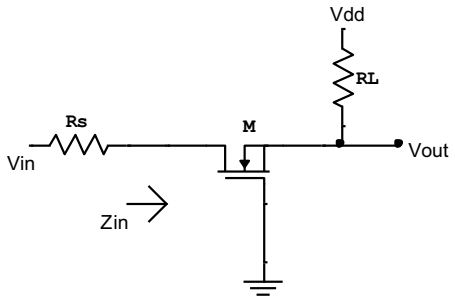

FIGURE 3.5: Common Gate (CG) topology

3.3.1 Noise Figure analysis of CG

CG topology has two sources of noise, source resistor and MOSFET channel noise. NF of CG is express using (3.13).

$$NF = 1 + \frac{\overline{V_n^2}}{|\alpha^2| A_v^2} \times \frac{1}{\overline{V_{RS}^2}} \tag{3.13}$$

Where, $\alpha = \frac{Z_{in}}{Z_{in} + R_S} = \frac{1/g_m}{1/g_m + R_S} = \frac{1}{1 + g_m R_S}$, $\overline{V_n^2} = \frac{4kT\gamma}{g_m}$, $\overline{V_{RS}^2} = 4kTR_s$, $A_v = g_m R_L$, so

$|\alpha^2|A_v^2 = g_m R_L \times \frac{Z_{in}}{Z_{in}+R_s} = \frac{R_L}{R_s+1/g_m}$ Substituting these value in (3.13) NF simplify as shown in (3.14)

$$NF = 1 + \frac{\left(\frac{4kT\gamma}{gm}\right)}{4kTR_s} + \frac{4kTR_L}{4kTR_s\left(\frac{R_L}{R_s+\frac{1}{g_m}}\right)^2} \quad (3.14)$$

At input impedance match $R_s = 1/g_m$ NF further simplify as

$$NF = 1 + \gamma + 4\frac{R_s}{R_L} \quad (3.15)$$

The NF of a CG topology can be calculating as (3.15) where, γ is process dependent noise parameter. Noise Figure of CG is improved by increasing transconductance (g_m) but it degrades wideband input matching. Here is the tradeoff to set g_m value for achieving low noise figure and wideband matching.

The effect of miller capacitance in CG can be reduced by using CG with CS cascode structure. Input impedance of CG with CS cascode structure is expressed as (3.16)

$$Z_{in} = 1/(g_m + g_{mb}) \quad (3.16)$$

Where, g_m and g_{mb} are transconductance of the transistors. Major drawbacks of the CG topology are low gain, higher NF at wideband matching and high power consumption [35, 36].

In literature work, used different hybrid topology with CG to achieve wideband matching, low NF and high power gain [21, 24, 37]. CG with positive feedback topology relaxes trancondutance (g_m) selection constraint for input matching. Positive feedback increase loop gain and reduce overdrive voltage due to that Linearity and NF performance is degrade [21]. In feedback path purposely uses inverting amplifier to enhance transconductance [37]. The negative feedback in CG reduces NF and power consumption but it has degraded stability of design. The positive-negative feedback gm boosted design approach has improved NF and gain without sacrificing linearity and input matching [37]. It has provide same power gain as positive feedback with half the power consumption. Various other techniques such as dual negative feedback [38] and noise cancellation [32] used with CG to improve performance of the LNA.

In the paper [39] used parallel common source with CG to decoupled tradeoff between input impedance matching and noise figure of the CG amplifier. With the CG various distortion cancellation techniques are used in [28, 40, 41, 33] to improve the linearity.

3.4 Feedback LNA Topologies

Negative feedback in LNA is widely used to achieve wideband input impedance matching with low NF. Various negative feedback LNA topologies are shown in Fig. 3.6. Lossless transformer as a feedback has best performance but it requires larger silicon area [42]. As a feedback network resistor, series RC, parallel RC and transistor are widely used. Negative feedback topology improves NF and input impedance matching of the design.

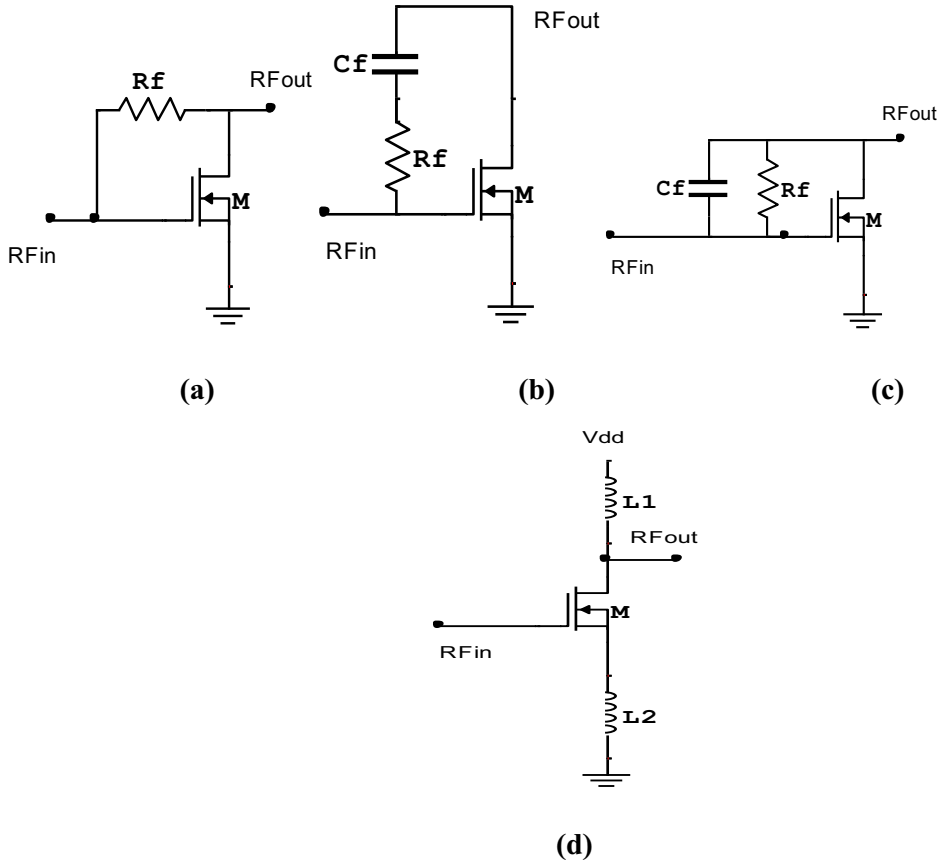

FIGURE 3.6: Feedback topologies a) resistive b) series RC c) parallel RC and d) transformer.

3.4.1 Resistive Feedback LNA Topology

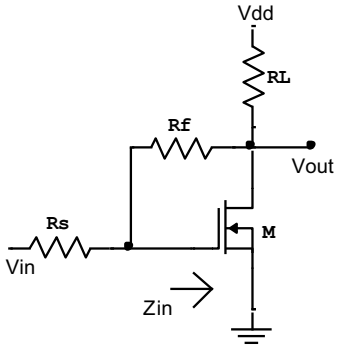

FIGURE 3.7: Resistive feedback common source (CS) topology.

GAIN ANALYSIS: Gain of resistive feedback CS topology can be derived from its AC equivalent circuit as shown in Fig. 3.8.

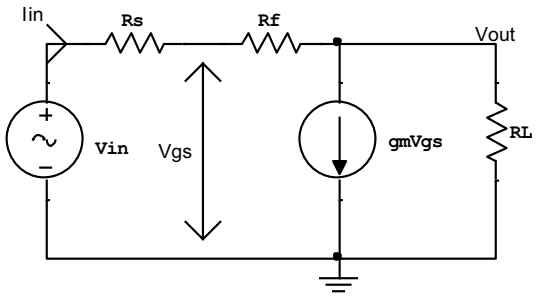

FIGURE 3.8: AC equivalent circuit of resistive feedback CS topology.

Applying KCL in input loop obtained input and output voltage relation

$$V_{in} = i_{in}(R_s + R_F) + V_{out} \tag{3.17}$$

$$V_{out} = (i_{in} - g_m V_{gs})R_L \tag{3.18}$$

$$V_{gs} = i_{in}R_F + V_{out} \tag{3.19}$$

From the above equations gain of resistive feedback common source amplifier can be expressed as

$$A_{v,tot} = \frac{V_{out}}{V_{in}} = \frac{R_L(1-g_m R_L)}{R_s+R_F+R_L+g_m R_s R_L} \tag{3.20}$$

Where, R_S, R_F and R_L are source, feedback and load resistor respectively. If $R_F \gg R_s$ & $g_m R_F \gg 1$ then gain equation can be simplify as

$$A_{v,tot} = \frac{-g_m R_L}{R_s+R_F+R_L+g_m R_s R_L} \cong -g_m R_L \tag{3.21}$$

Input impedance for resistive feedback common source amplifier is expressed as shown in (3.22).

$$Z_{in} = \frac{R_F + R_L}{1 + g_m R_L} \tag{3.22}$$

NOISE FIGURE ANALYSIS: Resistive feedback amplifier has three sources of noise, such as source resistor, feedback resistor and MOSFET. Total noise is addition of all individual source noise. MOSFET channel and source resistor thermal noise can be express as (3.23) and (3.24).

$$\overline{I_{nd}^2} = 4kT\gamma g_m \Delta f \tag{3.23}$$

$$\overline{V_{RS}^2} = 4kTR_s \Delta f \tag{3.24}$$

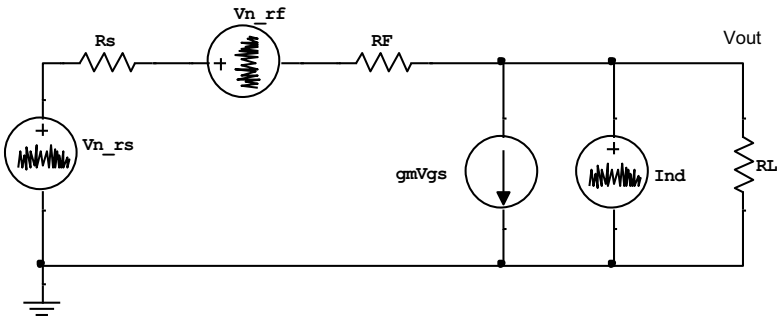

FIGURE 3.9: AC equivalent circuit with noise sources of resistive feedback CS.

Noise figure of resistive feedback common source LNA topology is expressed as

$$NF = \frac{\overline{V_{n,RS,out}^2} + \overline{V_{n,RF,out}^2} + \overline{V_{n,d,out}^2}}{A_v^2 \overline{V_{n,RS}^2}} \tag{3.25}$$

Output noise due to source resistor

$$\overline{V_{n,RS,out}^2} = A_v^2 \overline{V_{n,RS}^2} \tag{3.26}$$

Output noise due to feedback resistor: The output noise due to feedback resistor is obtain by keeping only feedback resistance noise source and replacing all others sources by zero value in Fig. 3.9.

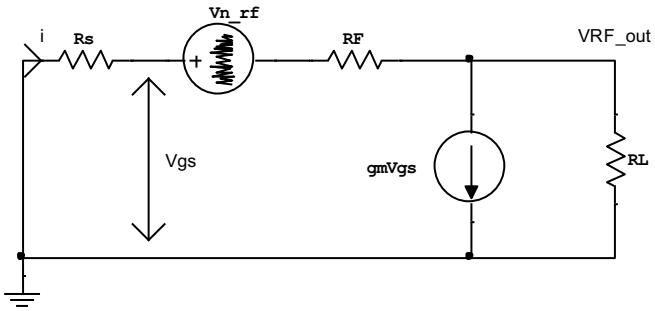

FIGURE 3.10: Feedback resistance noise of resistive feedback CS.

By applying KVL in input loop of Fig. 3.10.

$$V_{gs} = -iR_s = iR_F - V_{RF} + V_{RF,out} \tag{3.27}$$

$$V_{RF,out} = R_L(i - g_m V_{gs}) \tag{3.28}$$

$$V_{RF,out} = V_{RF}\frac{1}{1+\frac{R_S+R_F}{R_L(1+g_m R_S)}} = V_{RF}\frac{R_L}{R_F}(1+g_m R_s) \tag{3.29}$$

$$\overline{V_{n,RF,out}^2} = \overline{V_{n,RF}^2}\left[\frac{R_L}{R_F}(1+g_m R_s)\right]^2 \tag{3.30}$$

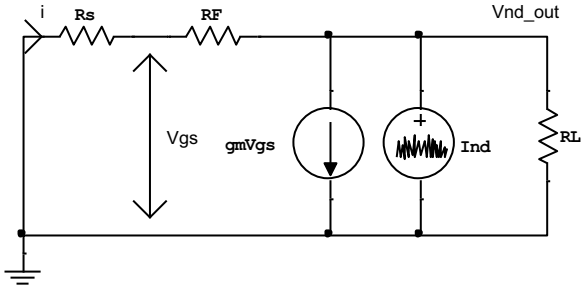

FIGURE 3.11: MOSFET drain current noise of resistive feedback CS.

Fig. 3.11 shows the output noise due to MOSFET channel noise only. Similar to feedback resistor, output noise due to MOSFET channel is expressed as (3.31)

$$\overline{V_{nd,out}^2} = \overline{I_{nd}^2}R_L^2 \tag{3.31}$$

By using (3.26), (3.30) and (3.31) values total NF is

$$NF = 1 + \frac{\overline{V_{n,RF}^2}\left[\frac{R_L}{R_F}(1+g_m R_s\right]^2}{A_v^2\overline{V_{n,Rs}^2}} + \frac{\overline{I_{nd}^2}R_L^2}{A_v^2\overline{V_{n,Rs}^2}} \tag{3.32}$$

Where, $A_v = -g_m R_L$ $\overline{V_{n,Rs}^2} = 4kTR_s\overline{V_{n,RF}^2} = 4kTR_F\overline{I_{n,d}^2} = 4kTR\gamma g_m$ putting these values in (3.32)

$$NF = 1 + \frac{R_S}{R_F}\left(1 + \frac{1}{g_m R_S}\right)^2 + \frac{\gamma}{g_m R_S} \quad (3.33)$$

Equation 3.33 shows noise figure of resistive feedback is inversely proposal to R_F and g_mR_s. Increasing feedback resistance value NF of the design is improved but it degrades input impedance matching. Here is trade-off between NF and input matching in resistive feedback topology. At higher frequency resistive feedback CS amplifier need gate inductor to tune out C_{gs} to improve gain at higher frequency.

Larger the value of feedback resistor reduces NF but it degrades linearity, input matching, and flat gain performance. Current reuse NMOS/PMOS pair inverter structure with resistive feedback is used in [43, 44] to improve linearity. Drawback of this topology is low bandwidth and this design use auxiliary transistor for feed forward noise cancellation which increase power dissipation. Similar resistive feedback topologies are used in [32, 45, 13] to achieve wideband better performance using noise and distortion cancellation techniques. In the papers [46, 47] used resistive feedback with NMOS/PMOS pair in a cross coupled fashion for noise cancellation. The design achieved very low NF (NF min 1.43 dB). To improve NF in the design used large size transistors which degrade high frequency response due to increasing parasitic capacitance.

In resistive feedback parasitic capacitance degrade higher frequency response. Reactive feedback is used in literature to improve higher frequency response at a cost of larger silicon area requirement.

3.4.2 Reactive Feedback LNA Topology

In reactive feedback used series RC [48, 49, 50] or parallel RC [51, 52, 53] or series RLC [54] circuit as a feedback network. The LNA reported in [48] used series RC feedback as shown in Fig. 3.6(b) with series and shunt inductive peaking to achieve good bandwidth, good NF and flat gain, but this design has poor linearity.

The designed reported in [51, 52, 53] use parallel RC feedback as shown in Fig. 3.6(c) to achieve broadband operation (3.1–10.6 GHz) and improved NF but these designs also suffer from poor linearity.

The design reported in [54] has used series RLC feedback for wideband (3.1-10.6 GHz) operation. This design has used positive negative feedback to achieve low NF and improve input matching at a cost of higher power consumption.

Fig. 3.6(d) shows transformer feedback LNA topology [55, 56, 57]. The LNA reported in [57] used transformer feedback and current reuse to achieve low NF and low power consumption. Drawback of this design is to require larger silicon area and poor linearity.

3.4.3 Active Feedback LNA

In active feedback circuit [58] the input stage is a common source amplifier and the feedback stage is a common drain amplifier. A simple analysis of this circuit shows that transconductance of the common drain stage controls the input impedance, while transconductance of the common source amplifier contributes to the gain and NF of the overall LNA. Active feedback adds one more degree of freedom to set input impedance and NF independently of the design. The main disadvantage of this architecture is the relatively high power consumption due to addition of the feedback stage.

3.5 Filter LNA Topology

The band pass filter is use to resonant at entire band to provide wideband matching [59]. Filter LNA has good performance while dissipating low power. Various types of filters are used like three-section band pass Chebyshev filter [60], Miller effect input matching filter [61], LC filter, dual RLC filter, high pass filter [62], π LC filter [63] and transformer based wideband input matching circuit of such LNAs.

CS inductive degeneration stage with filter input matching circuit is used to achieve good NF, Low power consumption, high gain and wideband input matching in the literature [60, 64]. Due to large value of inductors, filter topology require off chip components.

The LNA presented in [61] for 3–5 GHz wideband use gate inductive peaking in addition to a source degeneration inductor. Here exploitation of Miller effect is providing wideband matching. This approach reduce NF (≤2.3 dB) and chip area with the cost of poor linearity

(IIP3= −13 dBm). The LNA (0.18μm CMOS) [64] provides wideband operation (3.1–10.6 GHz) with low power consumption (9.4 mW) by using current reuse at a cost poor linearity.

3.6 Distributed Amplifier LNA Topology

Distributed amplifiers are widely used in wideband LNA design [65]. Several stages of common source distributed amplifier structure consume more power and require larger silicon area. Wideband frequency response is achieved by forming transmission lines by combining the parasitic capacitances of transistor with inductors. The DAs generally have flat gain, good linearity and inherently poor NF [35, 27, 65].

Power consumption in DA can be reduced by using current reuse techniques or low voltage. In [66], a low power LNA (90 nm CMOS) implemented using two distributed amplifiers in a matrix formation with tapered transmission lines. This design is biased in moderate inversion to reduce the power dissipation (12.5 mW) and achieve 21 GHz bandwidth, 15.4 dB gain with cost of poor linearity (IIP3=-6dBm).

Various NF improvement techniques used in DAs to improve NF performance. In some DA replaces resistive termination with series RL circuit to reduce the thermal noise generated by terminating resistor. This technique requires two power supply, consuming more power and having poor input impedance matching.

DA is less attractive in portable and compact device receiver due to high power consumption and requires larger silicon area. DA is widely used in instrumentation and medical imaging applications [66, 67].

Zhang et al. design wideband LNA using DA topology to reduce power dissipation 9mW by biasing transistors in moderate inversion [65].

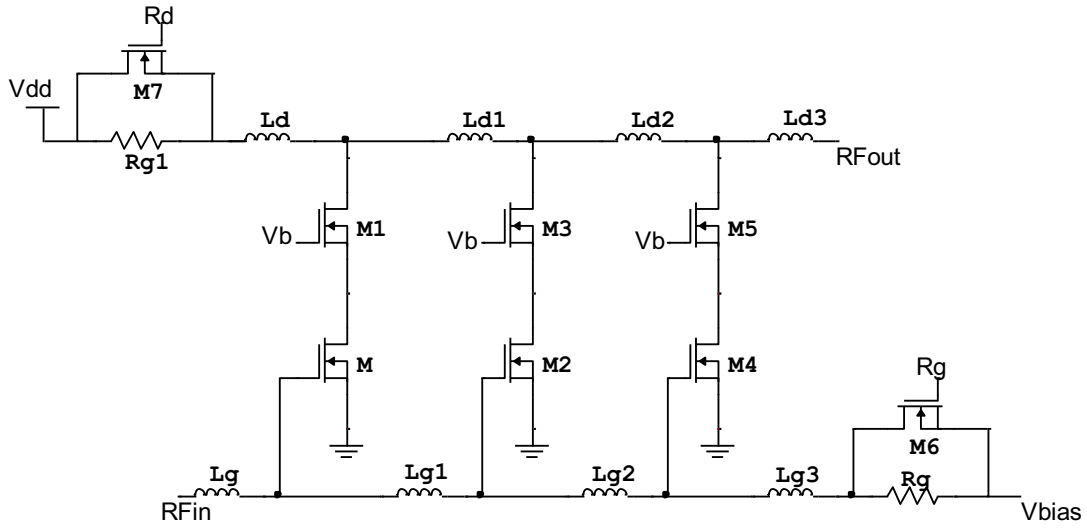

FIGURE 3.12: Cascode DA Schematic [65].

The schematic used in [65] is shown in Fig. 3.12. This topology used is called pseudo transmission line to increase bandwidth. Higher cut off frequency of DA is 1/(πRCg) where, R = (Lg/Cg)1/2 input impedance of DA to be set 50 Ω and Lg and Cg is gate inductance and capacitance respectively. Total power gain is summation of all stage gain by constructively adding all stages current.

Authors of this paper [65] have achieved low power consumption 9 mW but others parameters gain (8 dB), NF (10 dB) and consuming larger Si area are not satisfactory for future wireless receiver LNA.

Detail literature survey shows researchers have tried various hybrid wideband LNA topologies to relax tradeoff and improve performance. Still have scope in wideband LNA design to improve performance of future RF receiver. In this research proposed hybrid wideband LNA topologies and design for UWB and multi standards RF receiver.

To compare all LNA design on a single platform represented Figure of Merit (FOM) [79] as 3.34.

$$FOM = 20\,log_{10}\left(\frac{Gain(lin)\times BW(GHz)\times(IIP3(mW)}{(NF(dB)-1)\times Pd(mW)\times A(mm^2)}\right) \quad (3.34)$$

Where, BW is 3 dB bandwidth, IIP3, P_{DC}, NF and A are linearity, power dissipation, noise figure and area requirement of design.

TABLE 3.1: Summary of detail literature survey of the wideband LNA.

Source	CMOS Technology (um)	BW (GHz)	S21 (dB)	S11 (dB)	NF (dB)	IIP3 (dBm)	Pd (mW)	Area (mm^2)	Topology	FOM
JSSC-2004 [44]	0.25	0.002-1.6	13.7	<-8	2.4	0	35	0.075	Resisitive FB + NMOS/PMOS	20.18
JSSC-2004 [60]	0.18	2.3-9.2	9.3	<-10	4	-6.7	9	0.66	ID CS with input BPF	-3.04
JSSC-2005 [59]	0.18	2-4.6	9.8	<-9	2.3	-7	12.6	0.9	Series RC FB CS	-13.69
ICACT-2005 [62]	0.18	2.7-9.3	10	<-10	3.3	-0.3	14	-	Cascode with input HPF	
JSSE -2008 [64]	0.18	3.1-10.6	9.5	<-8.6	5-5.6	-13	9.4	-	Cascode with input filter and current reuse	
JSSCC-2006 [61]	0.18	3-5	<16	<-10.5	2.2	-9	7.68	0.629	CS with miller effect input matching filter	4.76
JSSC-2006 [65]	0.18	0.04-7	8.6	<-16	4.2	+3	9	1.16	Distributed cascode	9.62
JSSC-2007 [57]	0.13	3.1-10.6	15.1	<-9.9	2.5	-8.5	9	0.87	CS with reactive FB	9.3
JSSC-2007 [39]	0.18	3.1-10.6	9.7	<-11	4.7	-6.2	20	0.59	CG with noise cancellation	-8.3
JSSC-2007 [67]	0.18 SiGe	0.1-11	8	<-12	2.9	-3.55	21.6	0.76	Distributed cascode with BW enhancement	-0.23
ISSCC-2007 [68]	0.13	1-7	17	<-10	2.4	-4.1	25	0.019	Cascode + CD FB	44.91
JSSC-2008 [33]	0.13	0.8-2	14.5	-8.5	2.6	16	17.4	0.1	CG with noise and distortion cancellation	53.69
MJ-2008 [69]	0.18	5-6	20.5	-21.3	1.8-2.6	-6.2	2	-	Cascode + inter stage LC network	
ISSCC-2009 [37]	0.18	0.3-0.92	21		2	-3.2	3.6	-	Differential CG + C Cross coupling	
ISSCC-2009 [7]	0.13	3.1-10.6	15	-12	≤4.5	-12.5	26	0.435	Weighted distributed cascode	-9.45
TCAS-II -2010 [51]	0.18	3.1-10.6	13.9	<-9.4	4.7	-8.5	14.4	0.46	Parallel RC FB	0.51
MTT-s 2010 [63]	0.09	3.1-10.6	10.5	-10	3.2	4	21.6	0.139	Cs + Π input filter	30.1
MTT-S 2010 [70]	0.18	31.-10.6	13	-8.6	4.68	-12	10.34	-	CS + RLC input filter	
RFIC 2010 [66]	0.09	21	15.4		6	-6.6	12.5	0.41	Distributed CS + tapered transmission line	15.87
MTT-2011 [71]	0.09	0.01-1.77	23	<-10	2	-2.85	2.8	0.03	Differential CG + multiple	66.72

									feedback	
IET MAP 2012 [72]	0.18	2.4-11.2	14.8		3.9	-11.5	3.4	-	CG + current reuse	
MTT-2012 [73]	0.13	0.6-3	42v	<-8	3	-14	30	1.5	Pseudo differential + resistive FB	-17.48
IJEC-2012 [74]	0.18	3.1-10.6	15	<-11	3.5-3.9	6.4	16.2	0.39	Inverter with FB	35.66
MWCL-2012 [75]	0.065	0.01-2.8	32v		1	-13.6	40	-	Cascode + active –C element	
TCAS-II-2013 [76]	0.18	0-1.3	10	<-10	3	+7.5	18	0.07	Cascode + active feedback	29.25
IJMST-2013 [77]	0.18	2.5-16	11	<-7	3.3	-5	20	0.18	RC FB CS + current reuse	16.25
IJEC-2015 [78]	0.13	2.35-9.37	10.3	<-8	3.68	-4	9.97	0.39	CG current resue + noise cancelling	9.14
MJ-2015 [79]	0.13	3.5-5	14	<-15	3.5-3.9	4	21	0.31	Fully differential + active FB + Noise cancelling	14.62

JSSC-Journal of Solid State Circuit
ICACT-International Conference of Advanced Communication Technology
JSSE-Journal of Solid State Electron
ISSCC-IEEE International Solid State Circuit Conference
MJ- Elsevier Microelectronics Journal
TCAS-IEEE Transaction of Circuit and System
MTT-IEEE Transaction Microwave Theory
RFIC-IEEE proceeding of Radio Frequency Integrated Circuit
IET-IEEE Electronics Transaction
IJEC-International Journal of Electronics and Communication (AEU), Elsevier
IMCL-IEEE Microwave and Component Letter
IJMST-International Journal of Microwave Science and Technology

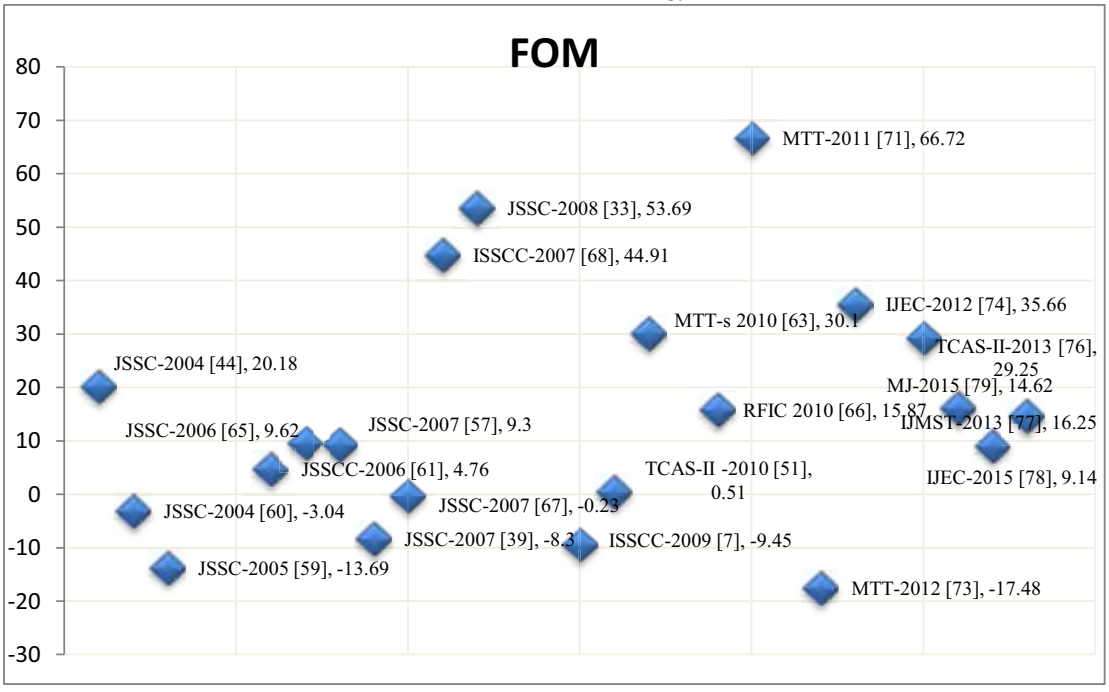

FIGURE 3.13: FOM of different LNAs design.

CHAPTER 4

Narrowband LNAs Design and Optimization

4.1 Inductive Degenerate Common Source (IDCS) LNA Topology

Inductive Degenerate Common Source (IDCS) LNA topology has the best performance compare to other topologies for narrowband applications. This chapter covers design of the Bluetooth receiver LNA using IDCS topology and also it design using Current Reuse (CR) topology for low power portable device applications. Another narrowband LNA is designed and optimized for Global Positioning System (GPS) receiver using IDCS and current reuse.

In the common source case, the input impedance is dominated by the gate-to-source capacitance (Cgs). So it is hard to achieve purely resistive impedance without input impedance matching network. Various input impedance matching circuit use resistor to match with source resistor. The resistive input matching circuit is add thermal noise. IDCS LNA topology achieve real impedance input matching without using resistor and improve NF of the design. IDCS topology use gate and source inductor to match input impedance. Gate inductor of IDCS dominates input capacitance of MOSFET Cgs by forming series LC circuit at desire frequency. Source inductor of IDCS produces real impedance to match source real impedance without use of resistor in design [55].

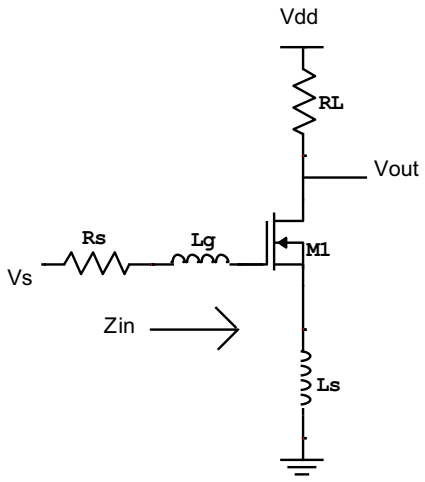

FIGURE 4.1: Inductive Degenerate Common Source (IDCS) LNA topology.

4.1.1 Input Impedance Analysis

Input impedance is the impedance between input node to ground as shown in Fig. 4.1. Ac equivalent circuit of the input stage of inductive degenerate CS is shown in Fig. 4.2 by replacing MOSFET by its ac equivalent model.

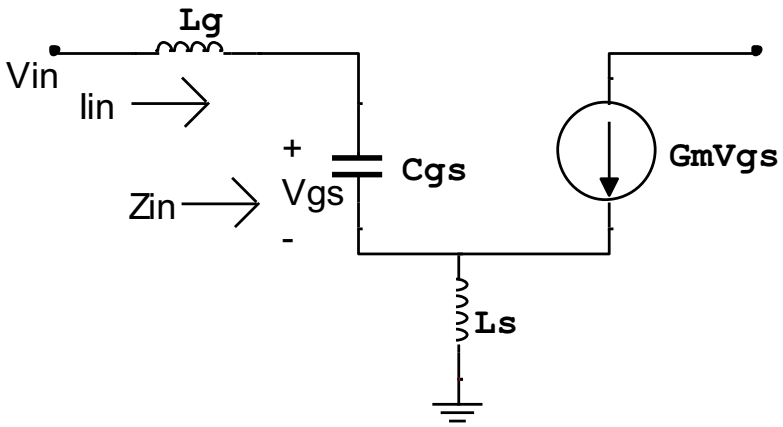

FIGURE 4.2: Inductive degenerate common source AC equivalent circuit.

Applying KVL in input loop of circuit shown in Fig. 4.2 input voltage is expressed in term of input current as shown in (4.1)

$$V_{in} = SL_g I_{in} + \frac{I_{in}}{SC_{gs}} + \left(I_{in} + G_m V_{gs}\right) SL_s \tag{4.1}$$

$$\frac{V_{in}}{I_{in}} = Z_{in} = S(L_g + L_s) + \frac{1}{SC_{gs}} + \frac{G_m L_s}{C_{gs}} \quad (4.2)$$

As shown in (4.2), input impedance of inductive degenerate is similar to series RLC circuit impedance. First, second and third terms of input impedance shown in (4.2) are inductive, capacitive and resistive impedance respectively. So, IDCS achieved resistive input impedance without using resistor. Resistive term (G_mL_S/C_{gs}) depend on trasconductance, source inductance and gate to source capacitance of MOSFET. Generated resistive impedance using degenerate inductor will not generate noise as real resistor so it minimize noise figure of the design.

For input match with 50 Ω Real (Z_{in})=50Ω = $\frac{G_m L_s}{C_{gs}}$ Input matching frequency can be found by Imaginary(Z_{in})=0

$$w(L_g + L_s) + \frac{1}{wC_{gs}} = 0 \quad (4.3)$$

$$\omega_o = \frac{1}{\sqrt{C_{gs}(L_g + L_s)}} \quad (4.4)$$

4.1.2 Gain Analysis

Input impedance of the IDCS topology is expressed as (4.5)

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \quad (4.5)$$

Input impedance shows input impedance of IDCS look like series RLC circuit as shown in Fig. 4.3.

Q factor of series RLC circuit is define as $Q_s = \frac{\omega_o L}{R} = \frac{1}{\omega_o RC}$ and, hence voltage across capacitor (V_c) is $Q_s V_{in}$ where V_{in} is input voltage of RLC circuit. For the design input quality factor is defined as (4.6)

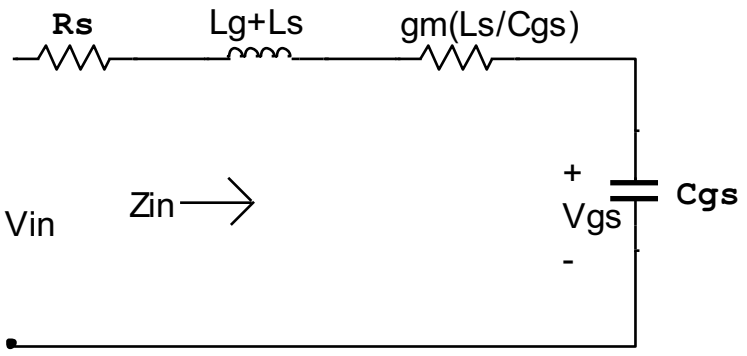

FIGURE 4.3: Input equivalent circuit of indcutive source degenerate CS LNA.

$$Q_{in} = \frac{\omega_o(L_g+L_s)}{R_s+\frac{g_m L_s}{C_{gs}}} = \frac{\omega_o(L_g+L_s)}{R_s+\omega_T L_s} \tag{4.6}$$

$$\therefore \omega_T \cong \frac{g_m}{C_{gs}} \tag{4.7}$$

Or using $Q_s = \frac{1}{\omega_o RC}$

$$Q_{in} = \frac{1}{\omega_o\left(R_s+\frac{g_m L_s}{C_{gs}}\right)C_{gs}} \tag{4.8}$$

for match load $R_s = \frac{g_m L_s}{C_{gs}}$

$$Q_{in} = \frac{1}{2\omega_o R_s C_{gs}} \tag{4.9}$$

Gate to source voltage of input transistor (V_{gs}) in terms of input quality factor is

$$V_{gs} = Q_{in} V_{in} \tag{4.10}$$

Transconductance of the MOSFET is defined as (4.11)

$$g_m = \frac{I_{out}}{V_{gs}} \tag{4.11}$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{V_{gs} g_m}{V_{in}} = Q_{in} g_m \tag{4.12}$$

$$G_m = Q_{in} g_m \tag{4.13}$$

So, gain of IDCS topology in terms of quality factor is expressed as (4.14)

$$Gain = -G_m R_L = -Q_{in} g_m R_L \tag{4.14}$$

4.1.3 Noise Performance Analysis

Noise figure is defined as

$$NF = \frac{Total\ noise\ power\ at\ output}{Noise\ power\ at\ output\ due\ to\ input\ source}$$

This design has two noise source, source resistor noise and MOSFET channel noise. Noise figure of the design is articulated as (4.15)

$$NF = 1 + \frac{\overline{V_{nD,out}^2}}{\overline{V_{nRS,out}^2}} \tag{4.15}$$

Where MOSFET noise can be modeled as

$$\overline{V_{nD,out}^2} = \overline{\iota_{nD}^2} R_L^2 \tag{4.16}$$

$$\overline{\iota_{nD}^2} = 4kT\gamma g_m \Delta f \tag{4.17}$$

Where, k is Boltsman, T is Temperature, γ is noise parameter of MOSFET, g_m is transconductance and Δf is bandwidth.

Output noise due to source resistor is expressed as (4.18)

$$\overline{V_{nRS,out}^2} = \overline{V_{nRS}^2} R_L^2 G_m^2 \tag{4.18}$$

Where, $\overline{V_{nRS}^2} = 4kTR_s\Delta f \& G_m = Q_{in} g_m$.By substituting (4.16) and (4.18) in (4.15) NF simplify as (4.19)

$$NF = 1 + \frac{\overline{\iota_{nD}^2} R_L^2}{\overline{V_{nRS}^2} R_L^2 Q_{in}^2 g_m^2} \tag{4.19}$$

$$NF = 1 + \frac{\gamma}{g_m R_s Q_{in}^2} \tag{4.20}$$

IDCS topology can be summarized from above equations as

- Very good NF value of this topology compare to other topology
- Narrow band matching can be achieved using Lg inductor
- Noise figure decrease with quality factors (NF with Q^2)

- The input quality factor value is dependent on L_g + L_s, but value of L_s is small compared to Lg and it can be neglected so input quality factor depend only on gate inductance L_g.

Noise figure of the design is improved by replacing load resistor R_L with drain inductor (L_D). This drain inductor form parallel tune circuit with load capacitor (C_L) where C_L is input capacitive impedance of the mixer. Value of this drain inductor is found by resonating parallel tune circuit at desire frequency.

$$\omega_o = \frac{1}{L_D C_L} \tag{4.21}$$

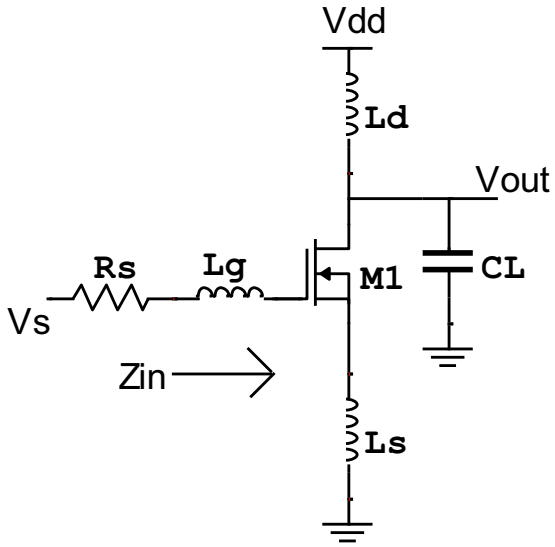

FIGURE 4.4: Inductive Load inductive source degenerate CS LNA.

This topology has poor reverse isolation between input and output due to miller capacitor. By use of cascode next stage of amplifier improve isolation without increase extra power consumption. In the Fig. 4.5 shows ID common source cascode inductive load LNA topology.

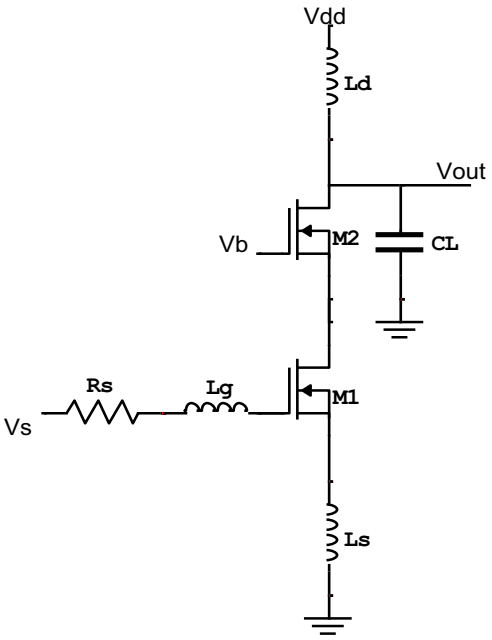

FIGURE 4.5: Cascode ID common source LNA.

4.2 Bias Circuit Design

The resistive bias is the simple bias circuit for an amplifier as shown in Fig. 4.6.

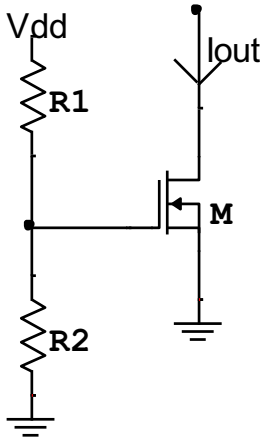

FIGURE 4.6: Resistive bias circuit.

DC current in saturation region is expressed as (4.22)

$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right)^2 \quad (4.22)$$

Equation 4.22 shows DC current dependent on various parameters like supply, process and temperature. Overdrive voltage is function of supply and threshold voltage. Supply and threshold voltage are dependent on PVT variation which make gate overdrive voltage fluctuation so, DC current is no more constant.

To make DC constant, widely used bias circuit is Copying current as shown in Fig. 4.7.

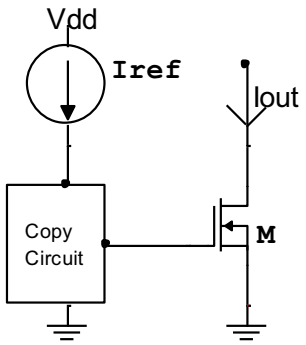

FIGURE 4.7: Current copying bias.

As we know $V_{gs} = f^{-1}(I_d)$, if it is biased at I_{ref}, then it produces $V_{gs} = f^{-1}(I_{ref})$. if we use V_{gs} voltage as gate bias of MOSFET then its produce output current $I_{out} = ff^{-1}(I_{ref}) = I_{ref}$. Current copy circuit is designed by using MOSFET operate in saturation region to work as constant current. Copying current bias circuit is called current mirror bias as shown in Fig. 4.8 and it widely used as bias circuit in analog circuit design.

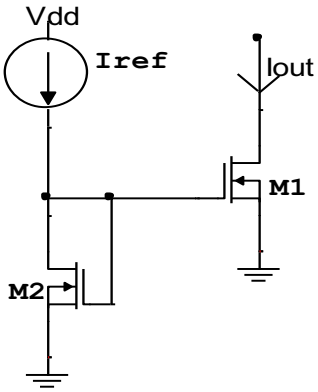

FIGURE 4.8: Current Mirror bias circuit.

Reference and output current of current bias circuit is expressed as

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 \tag{4.23}$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 \tag{4.24}$$

Output current is set using reference bias current using (4.25).

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \tag{4.25}$$

The key property of current mirror bias circuit is that it can set constant output current and make it independent of process and temperature. Considering saturation region modulation co efficient, currents can be found as (4.26) and (4.27).

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2}) \tag{4.26}$$

$$I_{OUT} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1}) \tag{4.27}$$

And hence

$$\frac{I_{REF}}{I_{OUT}} = \frac{(W/L)_2}{(W/L)_1}\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \tag{4.28}$$

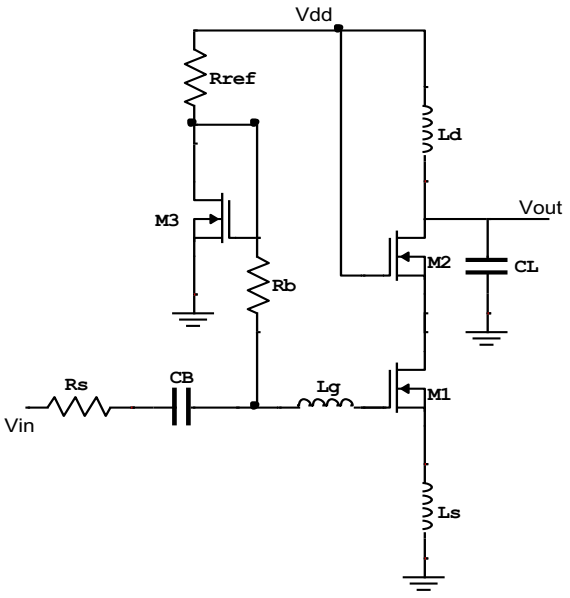

FIGURE 4.9: Inductive degenerate common source LNA topology with current mirror bias.

Inductor degenerate common source LNA topology with current mirror bias circuit is shown in Fig. 4.9.

Gate and source inductors are used to match impedance at desire frequency. Aspect ratio of MOSFET M1 and M2 decide gain of the design. MOSFET M3 is used for current mirror bias circuit to set bias current with Rref and Rb. Higher the value of Rref and Rb lesser will be thermal noise. Value of drain inductor with load capacitor is to set such that to resonance at desire frequency will improve gain and output matching. CB and Co are DC coupling capacitors at input and output respectively [80].

4.3 Bluetooth Receiver LNA Design using IDCS Topology

Bluetooth technology is widely used to create wireless Person Area Network (PAN) due to good data rate, good enough coverage range and simplicity in design. Bluetooth technology is using 2.4 GHz frequency for communication.

4.3.1 LNA Specifications for Bluetooth Receiver

NOISE FIGURE: The noise floor of the receiver express as

Noise floor = 10log(KT)+10log(BW)+NF=-174+10log(BW)+NF

Where K is Boltzmann constant, T is the absolute temperature, NF is the receiver noise figure, and BW is the channel selection filter bandwidth. To achieve the specified BER, certain SNRmin must be achieved. The SNR-BER curve is obtained from baseband system level simulations. The receiver sensitivity can be expressed in terms of SNRmin and noise floor as follows;

Sensitivity = SNRmin + noise floor + margin

Several dBs of margin are taken to account for nullification of process, temperature and voltage and any other effects that are unaccounted. Hence, the required NF of receiver can be expressed as

NF = Sensitivity – SNRmin - (-174 + 10log(BW)) - margin

THIRD ORDER INTERCEPT POINT (IIP3): The IIP3 can derive from the two tone test. Roughly estimate to find require IIP3 value from the state that SNRmin must be greater than IM3 product. The effect of the IM3 product is similar to

the noise effect. Although this is a rough approximation, it gives a good idea about the requires system IIP3 without the need to run the actual tone simulation. Such a simulation can take very long time because of the two higher frequency tones used.

The input referred IM3 product can be expressed as:

$P_{IM3} = 3P_{int} - 2IIP3 < P_{sig} - SNR_{min}$

Where P_{int} and P_{sig} are the interferer and signal levels when the IM test is conducted. Therefore, the minimum receiver IIP3 is given by:

$IIP3 = 1/2(3P_{int} - P_{sig} + SNR_{min}) + margin$

Again, several dBs of margin are added to account for implementation loss.

NF OF BLUETOOTH RECEIVER: The require Bluetooth receiver sensitivity is -70dBm. To achieved 10^{-3} BER require SNR_{min} is 13.6 dB. For 1MHz channel selection filter bandwidth and using 6 dB of margin, the require Bluetooth receiver NF is calculated as

$NF = -70 - 13.6 - (-174 + 10\log(10^6)) - 6 = 24.4$ dB

To support weak signals require good sensitivity to achieve -87 dBm sensitivity Bluetooth receiver require 7.4 dB NF.

IIP3 OF BLUETOOTH RECEIVER: In the intermodulation test, the receiver has to meet the 10^{-3} BER when the following signals are applied:

- The desired signal at frequency fo with a power level -64 dBm.
- Static sine wave signal at f_1 with a power level of -34 dBm.
- A Bluetooth modulation signal at f_2 with a power level of -34 dBm.

Such that f0 =2f1-f2 (f1 is closed to the signal than f2) and |f2-f1| = n x 1MHz, where n can be 3, 4 and 5. The system must fulfill one of these alternatives, substituting these values in equation using 6 dB margin:

$IIP3=1/2(3(-34) - (-64) + 13.6) + 6 = -6.2$ dBm

GAIN DISTRIBUTION: The first step to determine the specification of the receiver blocks is to determine require gain of each block. In order to relax the NF requirement of mixer and ADC block, front amplifier stage (LNA) gain should be maximized.

NF DISTRIBUTION: Distribute the NF among the receiver block such that the required overall system NF is met. For the cascaded stages overall system NF is calculated using the Friis equation. Where, LNA is the first stage of receiver. The Friis equation indicates that the noise contributed by each stage decreases as the gain of the preceding stages increases, implying that the first few stages in a cascaded are the most critical. Since the RF front-end gain is limited for to meet IIP3 requirement. NF of LNA dominate the overall system NF hence to keep minimum.

Bluetooth receiver LNA specification:

- Noise Figure (NF) < 3.5dB
- Power Gain (S_{21}) > 15dB
- IIP3 > -5dBm
- Input reflection coefficient (S_{11})<-15dB
- Output reflection coefficient(S_{22})< -10dB
- Centre frequency (f) = 2.4GHz
- Load Capacitance = 1pF

4.3.2 LNA Design Steps

First step of the design is to know process. 0.18µm CMOS process is used to design this LNA. 0.18µm CMOS technology have electron mobility μ_n=332.1cm^2/v-s, Oxide capacitor C_{ox} = 8.221X10^{-15}F/µm^2, so $\mu_n C_{ox}$=273.03µm, and channel length L=0.18µm.

- Optimum device width: In power optimization LNA design optimum value of quality factor express as [3]

$$Q_{opt,P_D} = |c|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|c|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \tag{4.29}$$

0.18 µm CMOS technology have correlation coefficient c=0.39, γ = 2, δ = 4 and α = 0.85. Quality factor value thus obtained is 3.9.

$$W_{M1,opt,P_D} = \frac{3}{2C_{ox}LQ_{L,opt,P_D}R_s w_0} \tag{4.30}$$

The operating frequency (f_0) is 2.4 GHz and ω_0=2X3.14X2.4GHz=15Grps. The value of R_s is 50Ω. Substituting all the value in (4.30) get power optimized MOSFET width is $W_{M1,opt,P_D} = 346.55\ \mu m$.

- Gate to Source Capacitance (Cgs): Cgs of MOSFET is modeled as

$$C_{gs1} = \frac{2}{3} C_{ox} X W_{M1} X L_{M1} \tag{4.31}$$

Substituting the values of C_{ox}, W_{M1} and L_{M1} in (4.31).$C_{gs1}$of this design is $C_{gs1} = 0.33\ pF$.

- Transconductanceof MOSFET(g_M) : The transconductance of the MOSFET is

$$g_{M1} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_{DM1}} \tag{4.32}$$

Where, for this design$I_{DM1} = 5mA$. So, $g_{M1} = 72.49mA/V$.

- Unity gain frequency (ω_T): Unity gain frequency of MOSFET is expressed as (4.33).

$$w_T = \frac{g_{M1}}{C_{gs1}} = 219.66Grps \tag{4.33}$$

- Power optimized design minimum noise figure ($F_{min,PD}$): In power optimized design minimum noise figure can be computed using (4.34) [3].

$$F_{min,P_D} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{w_0}{w_T}\right) \geq 1 + 1.62\left(\frac{w_0}{w_T}\right) \tag{4.34}$$

Where, $\gamma = 2$ and $\alpha = 1$ so, $F_{min,P_D} \approx 1.32dB$ .By increasing I_D, increases ω_T and decrease NF at the expense of more power.

- Starting value of Degeneration Inductor L_s: The value of this inductor is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology, which is technically about 10nH.

$$R_s = \frac{g_m L_s}{C_{gs}} = \omega_T L_s \tag{4.35}$$

So, $L_s = \frac{R_s}{w_T}$

- Evaluation of L_g: Lg of the IDCS structure is expressed as (4.36)

$$L_g = \frac{1}{w_o{}^2 C_{gs}} - L_s \tag{4.36}$$

- Evaluation of L_d: Here the value of C_L =1PF

$$L_d = \frac{1}{w_o{}^2 C_L} \tag{4.37}$$

- MOSFET Width (W): Width of M1 decides gain and input capacitance. M2 is used to reduce miller capacitance and improve isolation. If Width of M1 and M2 is equal then it can shared common area for drain and source. Size of M3 decides bias current and chose such that minimized power consumption.

- Bias resistor (Rb): Value of bias resistor is to be set large enough to neglect bias current noise. Value of the bias of the design is set Rb=2KΩ.

- Power dissipation: Power dissipation of design is found using total current consumption from given power supply voltage $P_d = V_{dd} \text{ X } I_d$. For the design P_d=1.8 X 5 X 10^{-3}= 9mW.

4.3.3 Schematic of the Bluetooth IDCS LNA

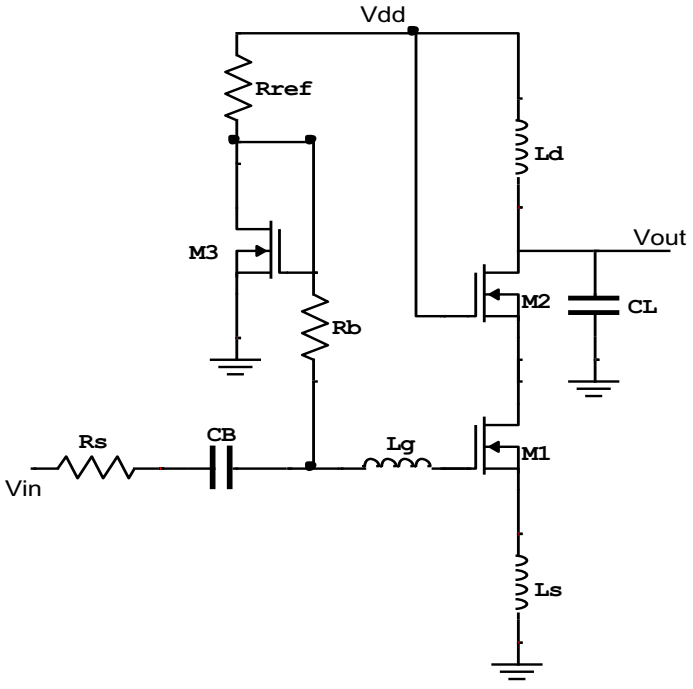

FIGURE 4.10: Bluetooth Inductive degenerate common source LNA schematic.

TABLE 4.1: Bluetooth LNA component values and its function.

Components	Experimentally optimized Value	Functionality
W_1, W_2	6X64 µm	Amplify the RF signal
W_3	5.2X10 µm	DC bias current mirror
Lg	4.28 nH	Input matching
Ls	0.14 nH	Input matching
Ld	1.82 nH	Output matching
CL	1 pF	Load Capacitance
CB	10 pF	DC blocking
Rb	2 KΩ	Reduce the input noise from DC bias circuit
Rref	2 KΩ	DC bias

Design components value and its function are given in Table 4.1.

LNA design is iterative process to find desired performances. Performance parameters of LNA have tradeoff among them. The LNA design is multi optimization problem.

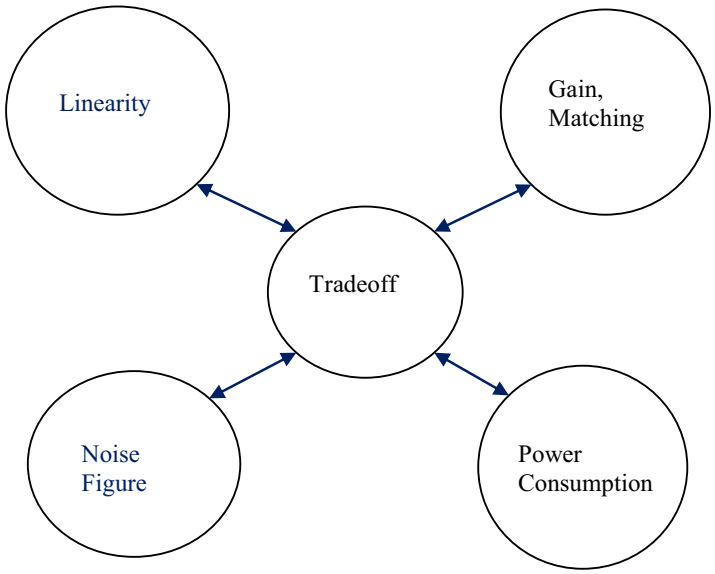

FIGURE 4.11: Performance tradeoff of LNA.

4.3.4 Design Optimization

In nanometer design, to find manual finding optimum design variables value manually is very difficult and impossible task due to complex mathematical model of MOSFET. To perform this complex time consuming task optimization algorithm is widely used to find optimum variables value. Fig. 4.11 shows design optimization flow chart.

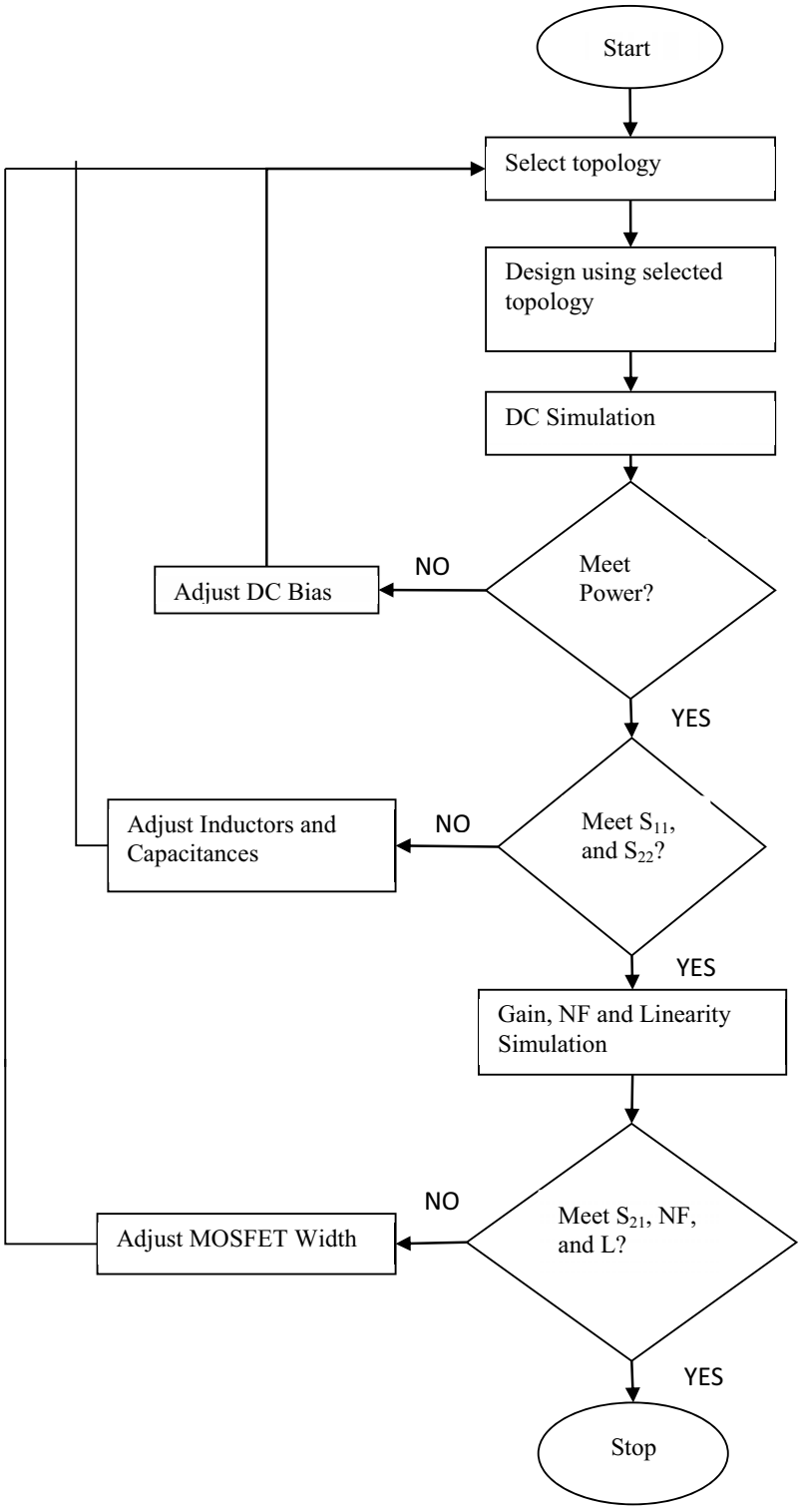

FIGURE 4.12: LNA design flow chart.

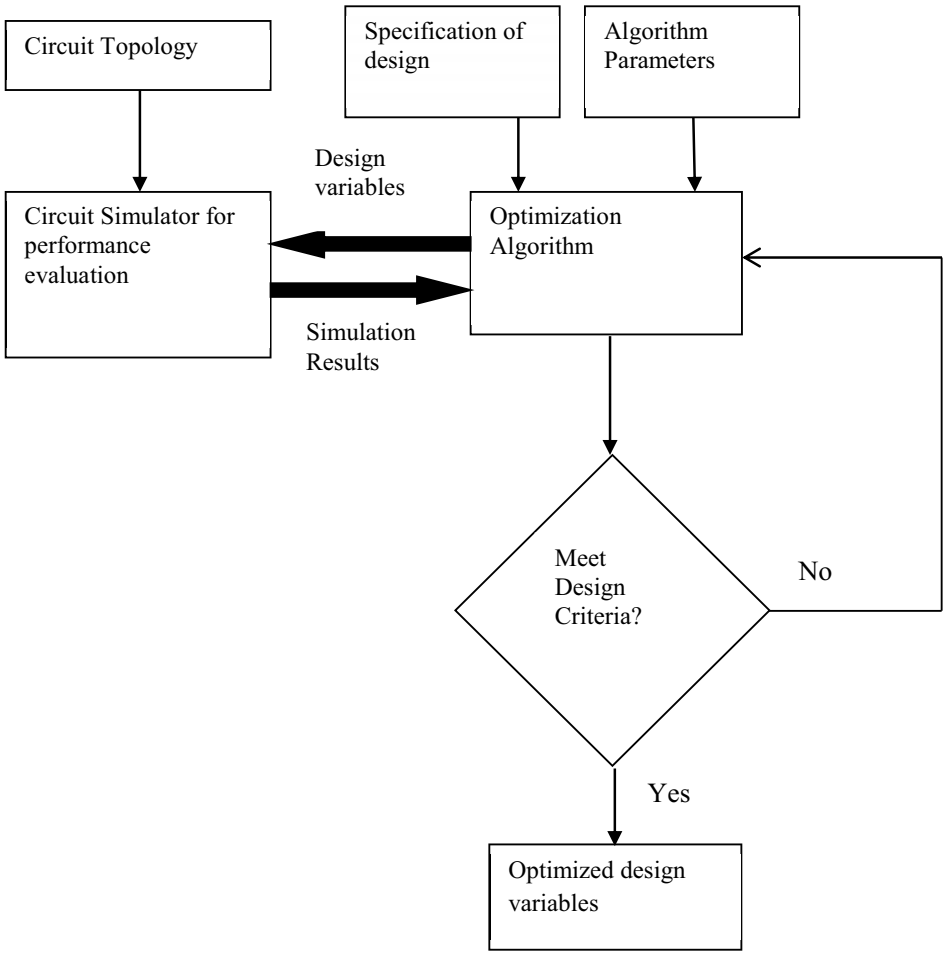

FIGURE 4.13: LNA design optimization flow chart.

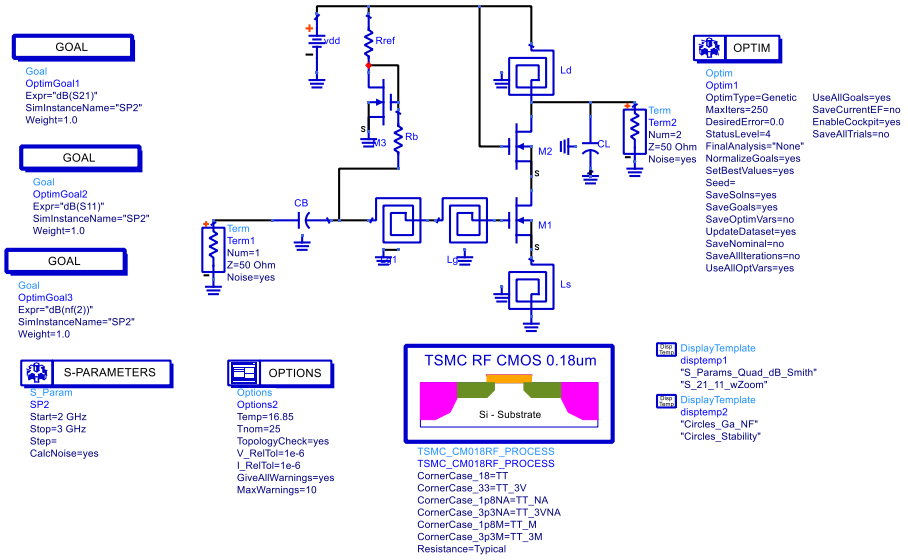

FIGURE 4.14: IDCS Bluetooth LNA ADS simulation schematic and optimization setup.

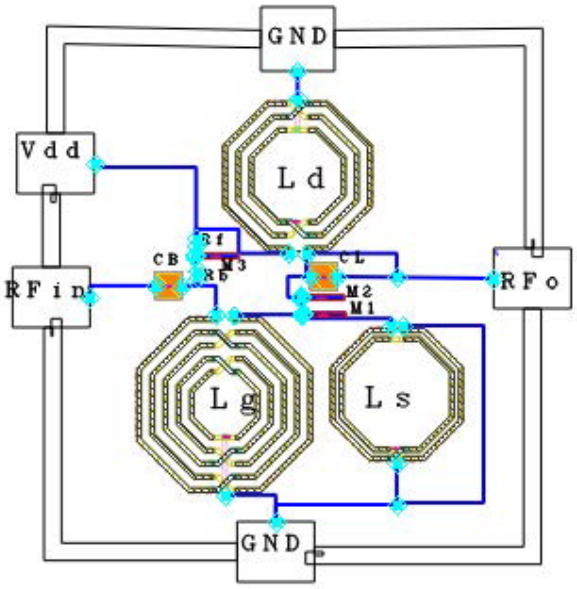

FIGURE 4.15: Layout of IDCS Bluetooth LNA.

4.3.5 Simulation Results and Discussion

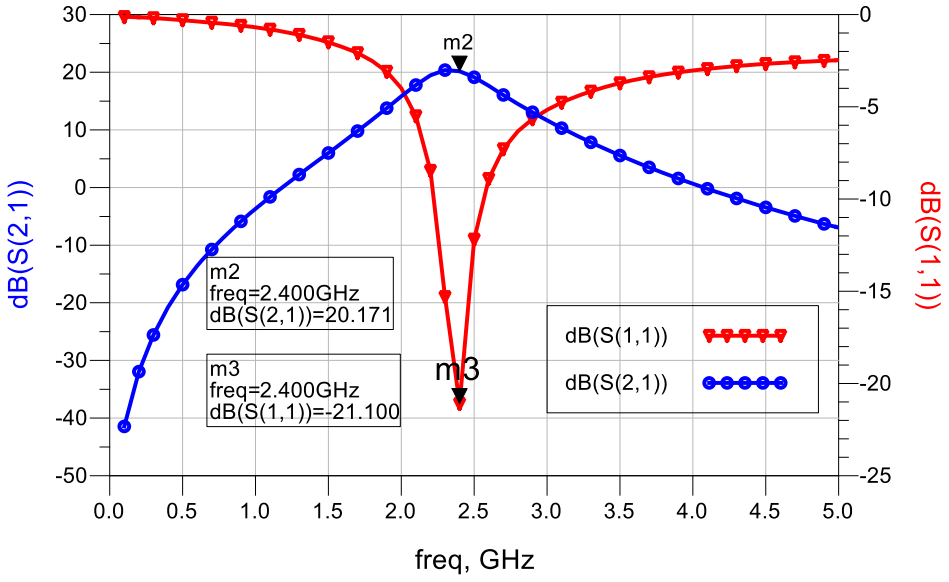

FIGURE 4.16: S_{21} and S_{11} Simulation results of Bluetooth IDCS LNA.

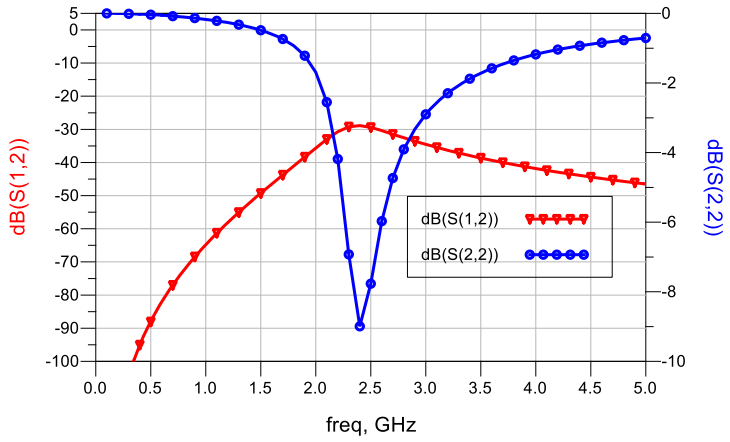

FIGURE 4.17: S_{12} and S_{22} Simulation results of Bluetooth IDCS LNA.

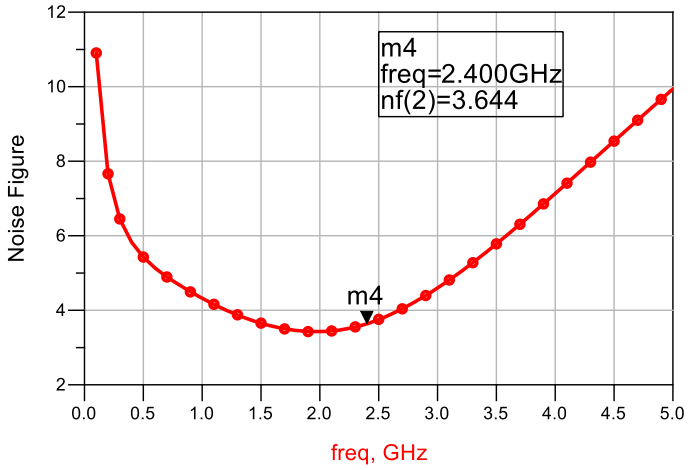

FIGURE 4.18: Noise Figure Simulation result of Bluetooth IDCS LNA.

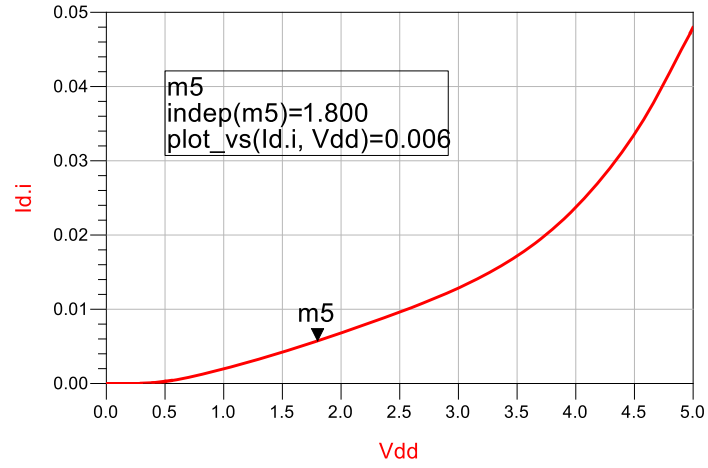

FIGURE 4.19: DC Simulation result Bluetooth IDCS LNA.

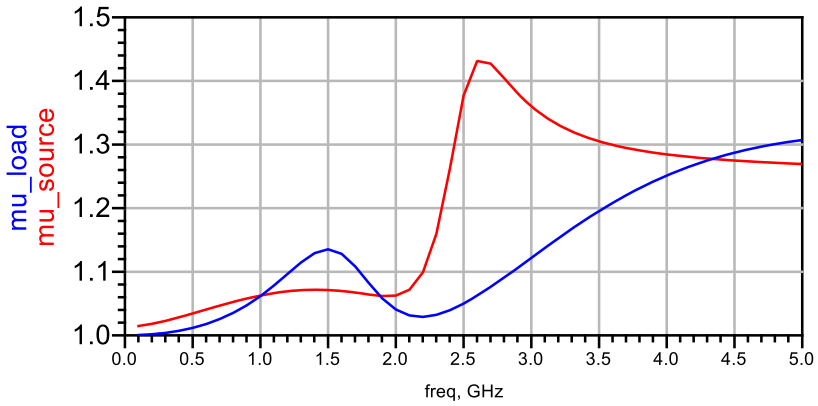

FIGURE 4.20: Stability factor simulation of Bluetooth IDCS LNA

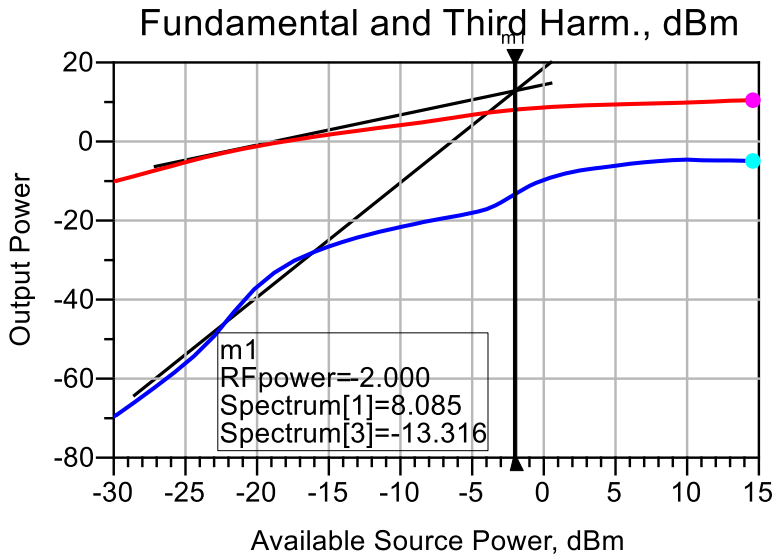

FIGURE 4.21: Harmonic simulation of Bluetooth IDCS LNA.

TABLE 4.2: Targeted and achieved performance of Bluetooth IDCS LNA.

Performance Parameters	Targeted specification	Achieved Result
Noise Figure (NF)	< 3.5 dB	3.56 dB
Power Gain (S_{21})	>15 dB	20.17 dB
S_{11}	<-15 dB	-21.0 dB
S_{12}	<-10 dB	-36.5 dB
S_{22}	<-10 dB	-9.0 dB
IIP3	>-5 dBm	-2.0 dBm
Power consumption	<10 mW	10.8 mW

Bluetooth IDCS LNA is designed using 0.18µm RFCMOS technology. The design is simulated using ADS RF circuit simulator. Fig. 4.16 shows achieved simulation results of power gain (S_{21}) and input reflection coefficient (S_{11}). The design has achieved more than 20 dB S_{21} and less than -21 dB S_{11} at desired frequency 2.4 GHz. Fig. 4.17 is shows

achieved good S_{12} andS_{22} are -29dB and -9dB respectively at desired frequency. Simulation results of NF and IIP3 are shown in Fig. 4.18 and Fig. 4.21 are 3.6 dB and -2 dBm respectively. DC simulation of the design is shown in Fig. 4.19 shows the design is consume 6mA total current including bias circuit from 1.8V supply. Total power consumption of the design is only 10.8 mW. Bluetooth IDCS LNA has achieved very good gain, input and output matching and linearity with tolerable noise figure. Fig. 4.20 is simulation result of stability and its shows stability coefficient is greater than one which means the design is unconditionally stable at desired frequency 2.4 GHz.

4.4 Bluetooth Receiver LNA Design using Current Reuse (CR) Topology

4.4.1 Bluetooth CRLNA Schematic

Current reuse topology is shown in Fig. 4.20. In CRLNA topology L1 and C1 are used to pass DC current and bypass AC signal. Inductor L2 couple output ac signal from first stage to gate of second stage. So in this topology same DC bias current is used in both the stages and due to reusing of DC current, it reduces power dissipation. Table 4.3 have design variables value and its function of the design.

TABLE 4.3: Bluetooth CRLNA Design variables value and its function.

Components	Value	Functionality
W_1, W_2	6x64µm	Amplify the RF signal
W_3	4.6x64µm	Second stage amplification
W_4	3.4x30µm	DC bias current mirror
Lg	3.67nH	Input matching
Ls	0.38nH	Input matching
Ld	1.82nH	Output matching
L1	2.68nH	Pass DC bias current
L2	5.8nH	Couple AC output signal to next stage
C1,C2	3.0 pF	AC Bypass
CB, Co	2.0 pF	DC Blocking
CL	1.0 pF	Load capacitance
Rb	2.0 KΩ	Reduce the input noise from DC bias circuit
Rref	2.0 KΩ	DC bias

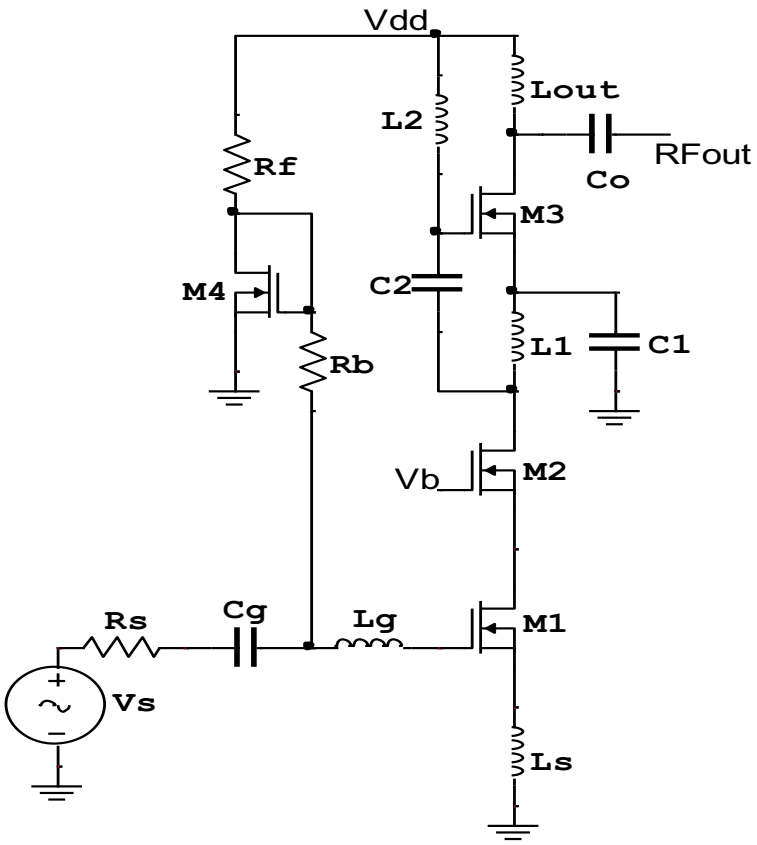

FIGURE 4.22: Bluetooth Current Reuse LNA (CRLNA) Schematic.

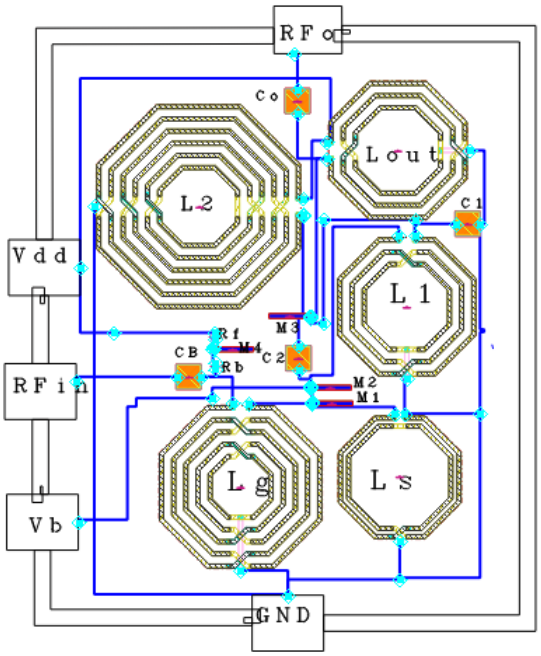

FIGURE 4.23: Layout of Bluetooth CRLNA

4.4.2 Simulation Results and Discussion

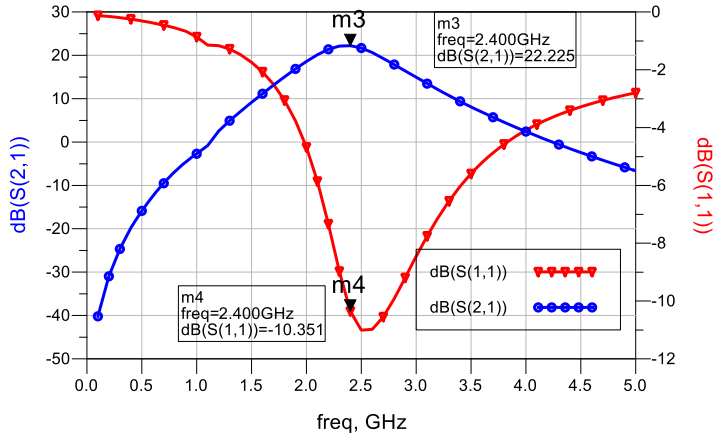

FIGURE 4.24: S_{21} and S_{11} simulation results of Bluetooth CRLNA.

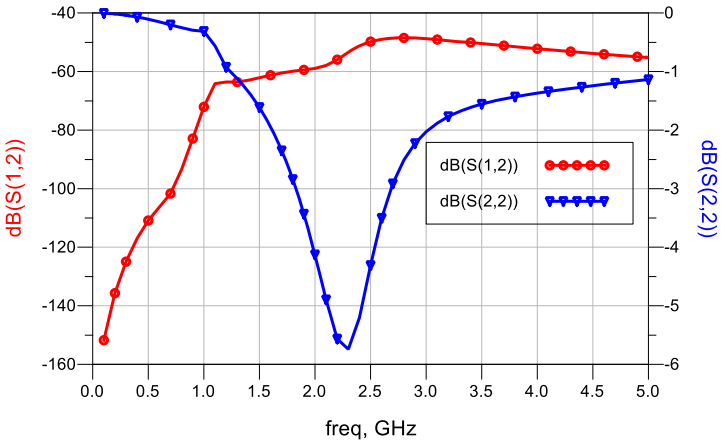

FIGURE 4.25: S_{12} and S_{22} Simulation results of Bluetooth CRLNA.

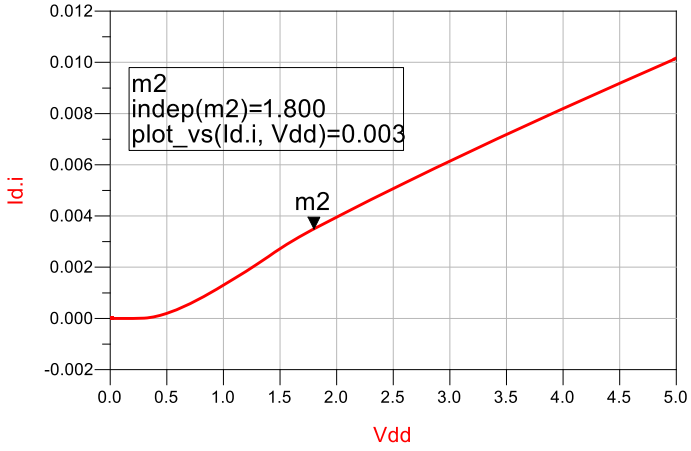

FIGURE 4.26: DC simulation of Bluetooth CRLNA.

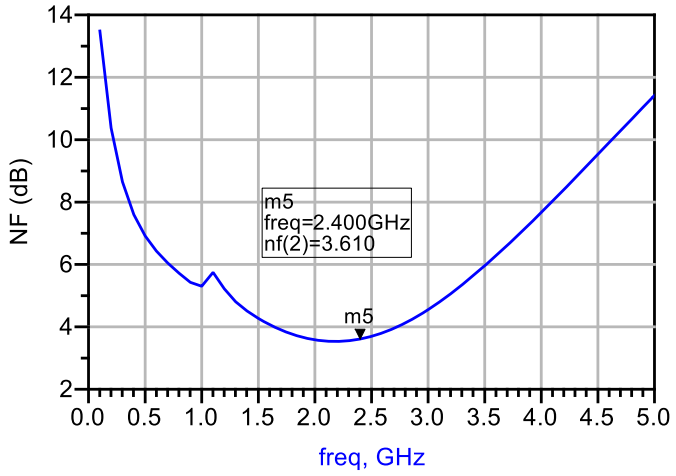

FIGURE 4.27: Noise Figure Simulation results of Bluetooth CRLNA.

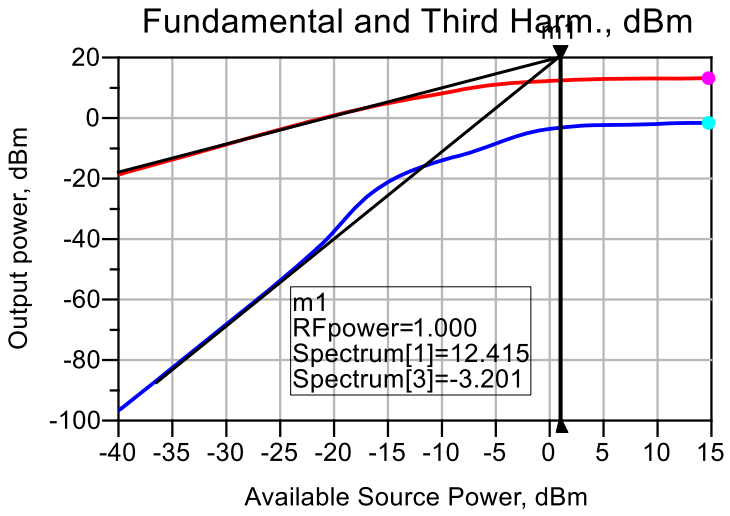

FIGURE 4.28: Harmonic Simulation of Bluetooth CRLNA.

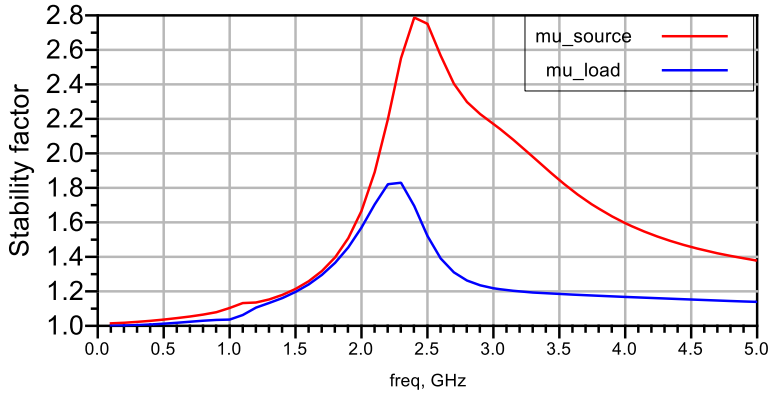

FIGURE 4.29: Stability factor simulation of Bluetooth CRLNA.

Simulation results of Bluetooth CRLNA shows achieved S_{21}, S_{11}, NF and IIP3 are 22.22 dB, -10 dB, 3.6 dB and 1 dBm respectively, with consuming only 3mA including bias

circuit current from 1.8 V supply. CRLNA achieve desired performaces with very low power consumption with a cost of higher si area. This CRLNA design is highly suitable for battery operated bluetooth receiver. Table 4.4 to summaries achieved perfromaces of proposed bluetooth LNAs with published work. To compare narrowband LNA here used Figure of Merit (FOM) is

$$FOM_N = 20log_{10}\frac{Gain\ (lin)\times IIP3(mW)}{(NF(dB)-1)\times Pd(mW)\times No.\ of\ coil} \quad (4.38)$$

TABLE 4.4. Bluetooth LNAs performance comparisons with literature works.

Design / Parameter	[81], 2006	[82], 2009	[83], 2008	[84], 2014	Design 1 Bluetooth IDCS LNA	Design 2 Bluetooth CRLNA
Technology (nm)	350	180	180	180	180	180
Frequency (GHz)	2.4	2.4	2.4	2.4	2.4	2.4
Power Gain (dB) (S_{21})	15	14.4	21.4 V	34.6 V	20.17	22.22
Input matching S_{11}	-32	-18.1	-19	-	-21	-10.3
Noise Figure (dB)	3.7	1.6	5.2	4.3	3.56	3.6
Power Consuption (mW)	33	0.96	1.3	19	10.8	5.4
IIP3(dBm)	-5	-9	-11	-10.6	-2	1
No. of inductor	4	4	1	1	3	5
FOM_N	10.4	3.72	-10.79	28.6	16.28	10.56

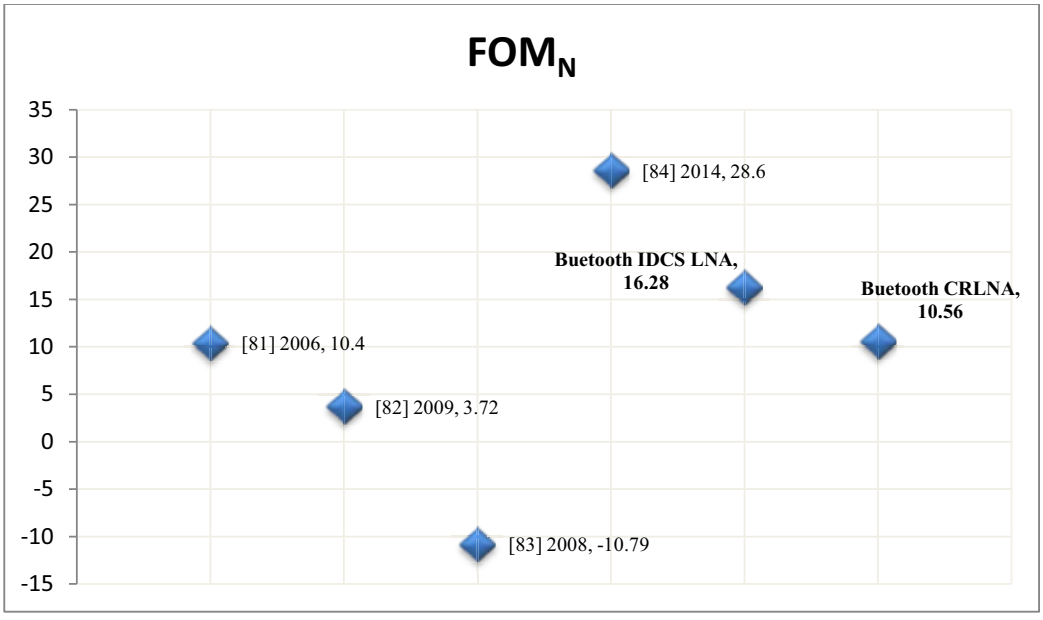

FIGURE 4.30: FOM of Published and proposed Bluetooth LNAs design.

4.5 GPS Receiver LNA Design

To receive very weak signal of Global Positioning System (GPS) require high sensitivity, high power gain and good linear receiver design.

4.5.1 GPS Receiver LNA Design using IDCS topology

The first LNA is design using IDCS topology for GPS receiver. GPS communication use 1.575 GHz frequency. Using LNA design and optimization flow obtained optimum component values of GPS LNA is given in Table 4.5.

TABLE 4.5: Design variables value of GPS IDCS LNA.

Components	Value	Components	Value	Components	Value
W_1	6.4x64 µm	Ls	0.14 nH	Rref	2 KΩ
W_2	6.5x64 µm	Ld	2.5 nH	Rb	2 KΩ
W_3	2.6X10 µm	CB	2 pF		
Lg	8.2 nH	Co	1 pF		

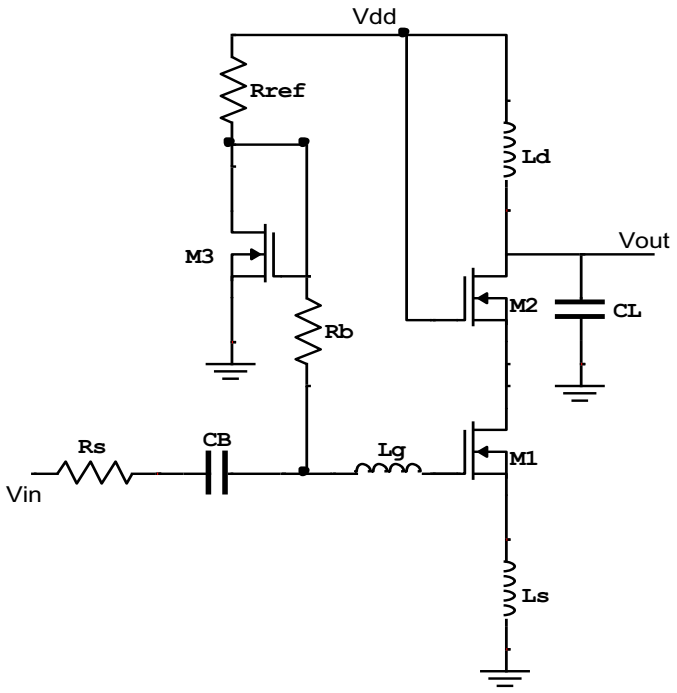

FIGURE 4.31: GPS IDCS LNA schematic.

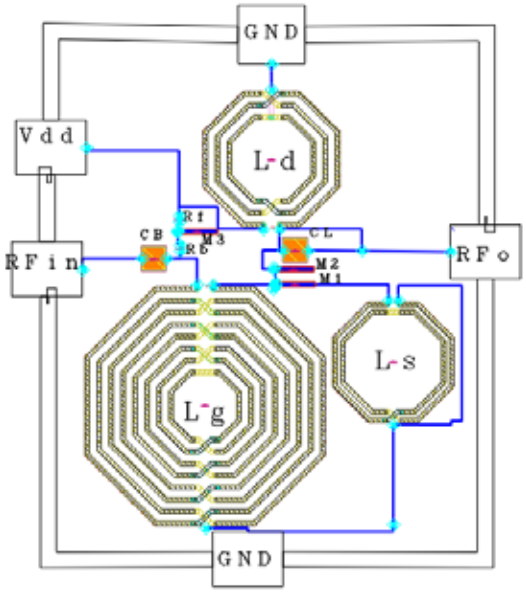

FIGURE 4.32: Layout of IDCS GPS LNA.

4.5.2 Simulation Results and Discussion of GPS IDCS LNA

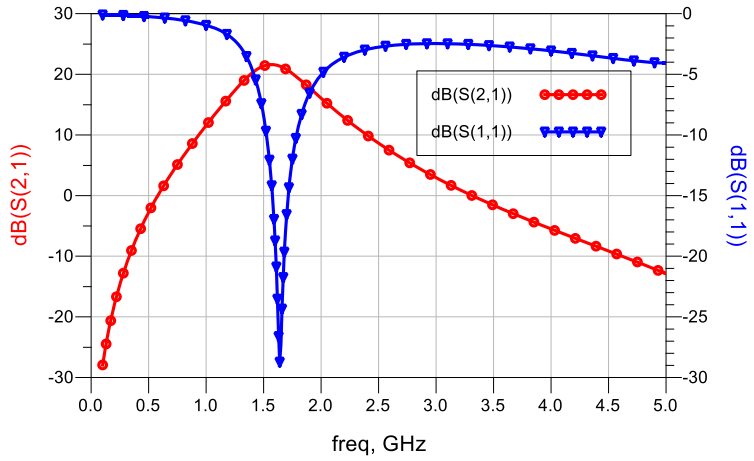

FIGURE 4.33: S_{21} and S_{11} simulation results of GPS IDCS LNA.

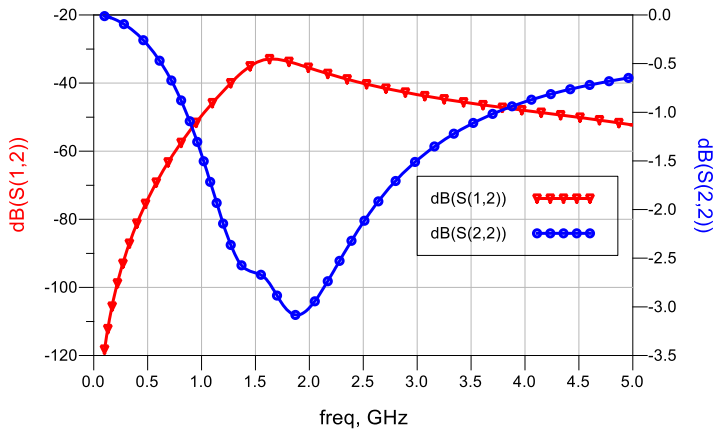

FIGURE 4.34: S_{12} and S_{22} simulation results of GPS IDCS LNA.

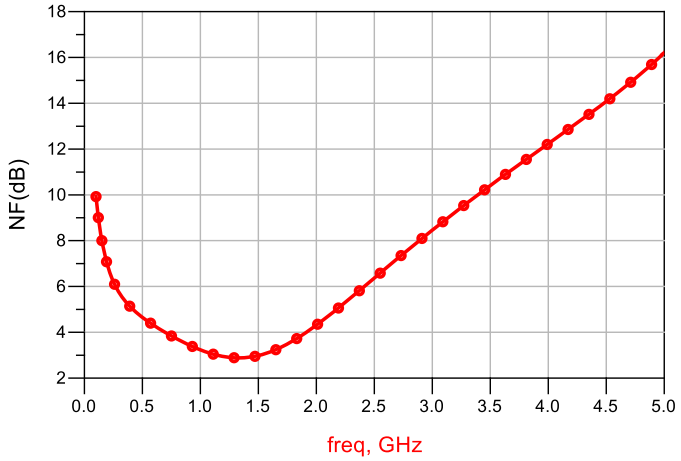

FIGURE 4.35: Noise Figure simulation results of GPS IDCS LNA.

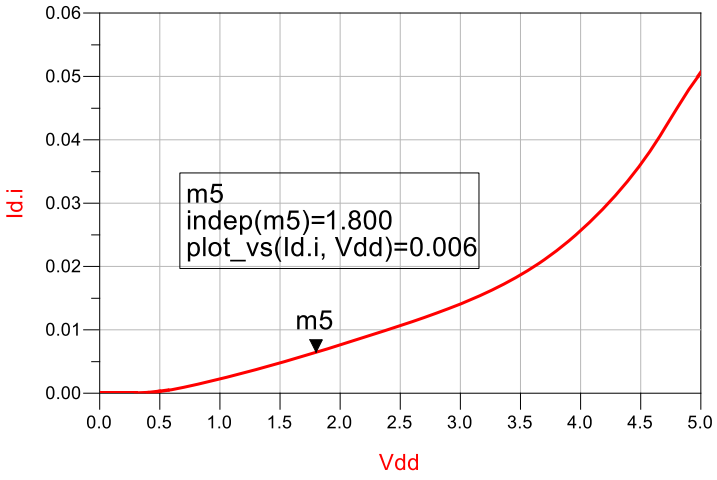

FIGURE 4.36: DC Simulation of GPS IDCS LNA.

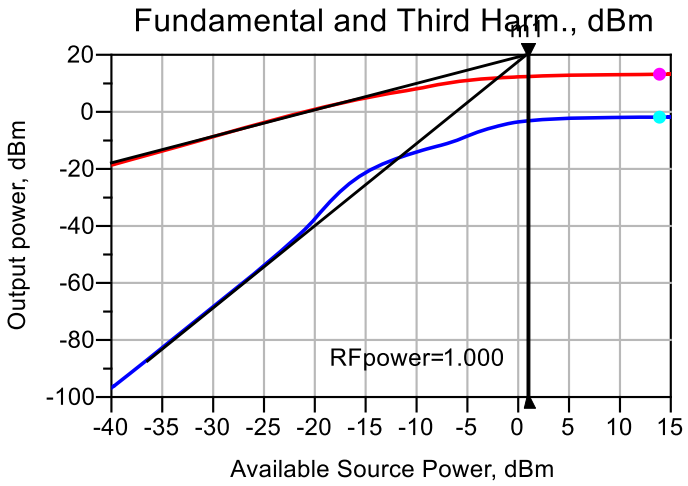

FIGURE 4.37: Harmonic simulation of GPS IDCS LNA.

GPS IDCS LNA design and simulate using RFCMOS 0.18 µm technology. Simulation results of GPS IDCS LNA shows achieved S_{21}, S_{11}, NF, IIP3 are 22dB, -25dB, 3dB and 1dBm respectively. Achieved results shows very good gain, very good input matching for maximum power transfer, low noise figure and good linearity. This design consume 6 mA current from 1.8V supply as is shown in Fig. 4.36.

4.5.3 GPS Receiver LNA Design using CR topology

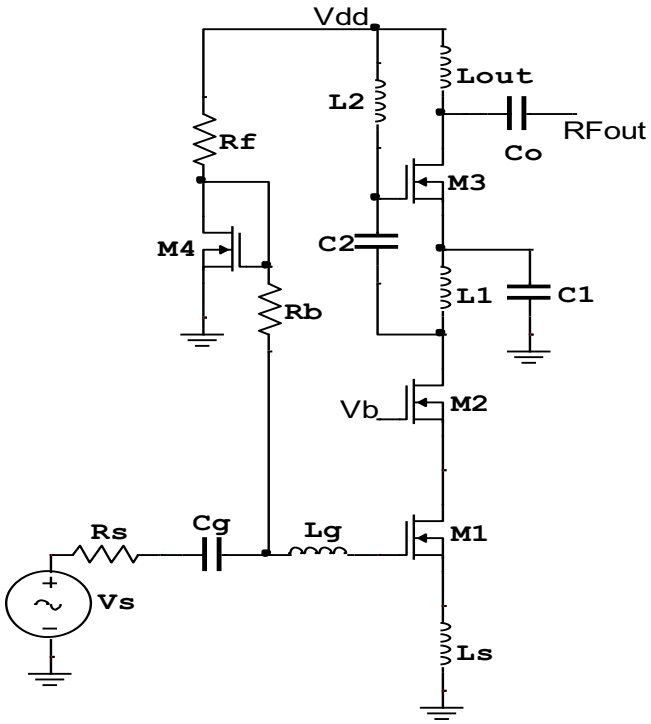

FIGURE 4.38: GPS Current Reuse LNA (CRLNA) Schematic.

TABLE 4.6: GPS CRLNA Design variables value and its function.

Components	Value	Functionality
W_1, W_2	6.4x64 µm	Amplify the RF signal
W_3	6.4x64 µm	Second stage amplification
W_4	2.6x10 µm	DC bias current mirror
Lg	7.1 nH	Input matching
Ls	0.14 nH	Input matching
Ld	2.05 nH	Output matching
L1	2.83 nH	Pass DC bias current
L2	2.8 nH	Couple AC output signal to next stage
C1,C2	3.0 pF	AC Bypass
CB, Co	2.0 pF	DC Blocking
CL	1.0 pF	Load capacitance
Rb	2.0 KΩ	Reduce the input noise from DC bias circuit
Rref	2.0 KΩ	DC bias

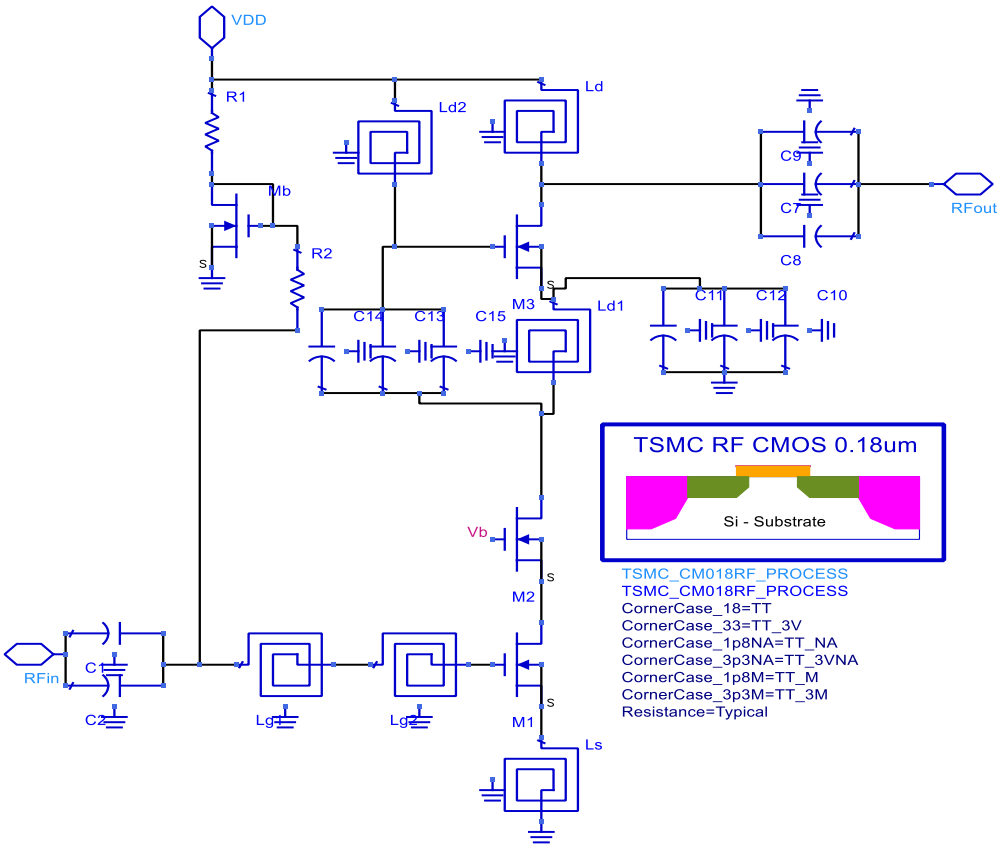

FIGURE 4.39: CRLNA GPS LNA ADS simulator schematic.

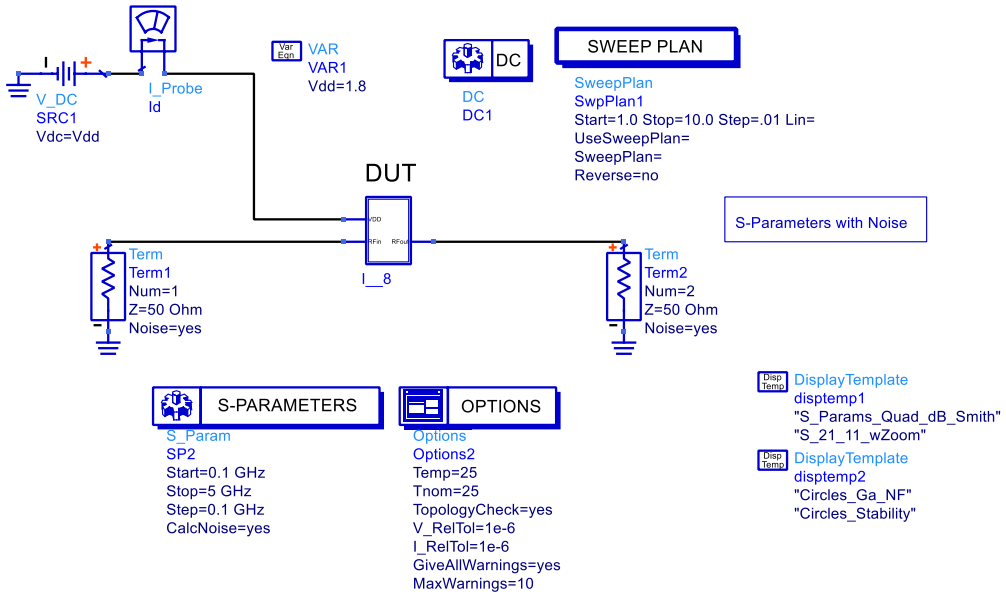

FIGURE 4.40: S parameters and Noise Performance simulation setup.

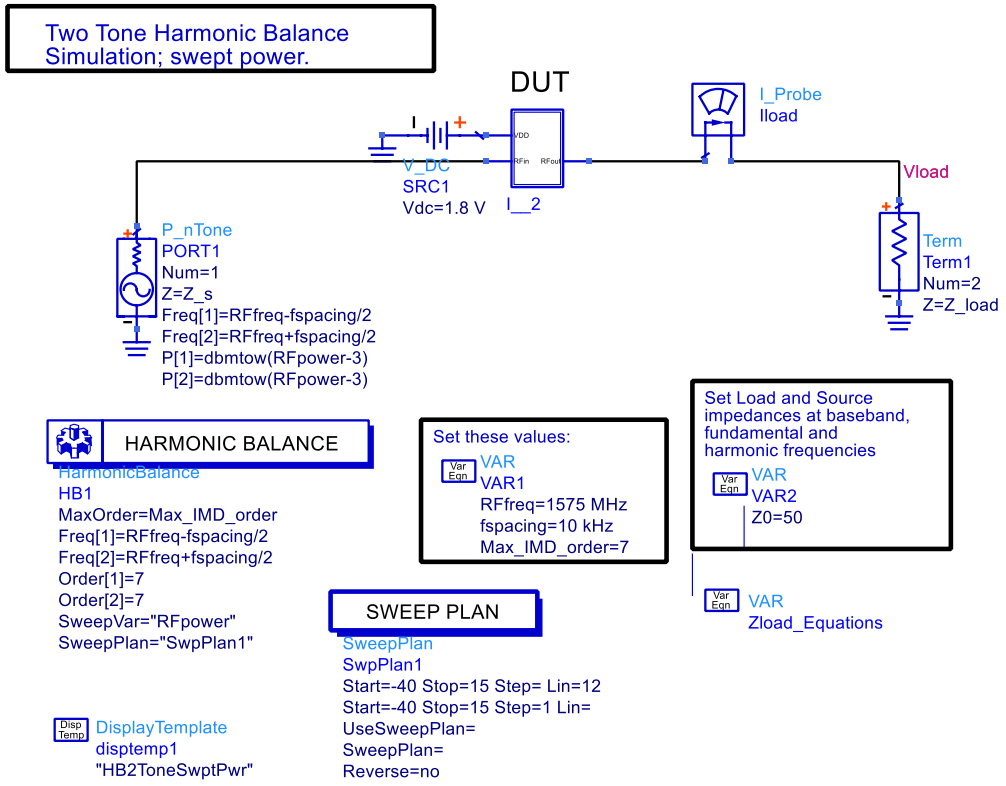

FIGURE 4.41: Harmonics balance simulation setup.

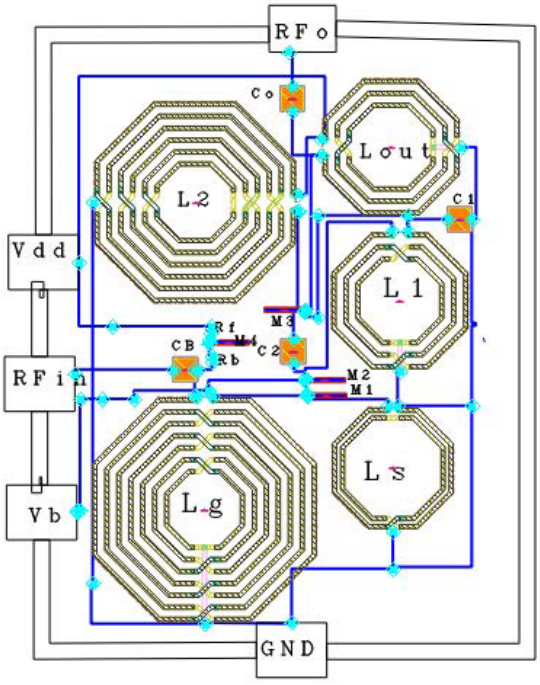

FIGURE 4.42: Layout of GPS CRLNA.

4.5.4 Simulation Results and Discussion of GPS CRLNA

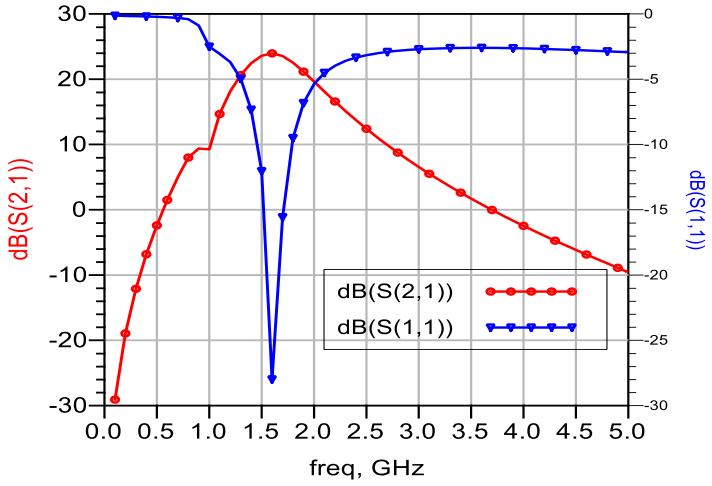

FIGURE 4.43: S_{21} and S_{11} simulation results of GPS CRLNA.

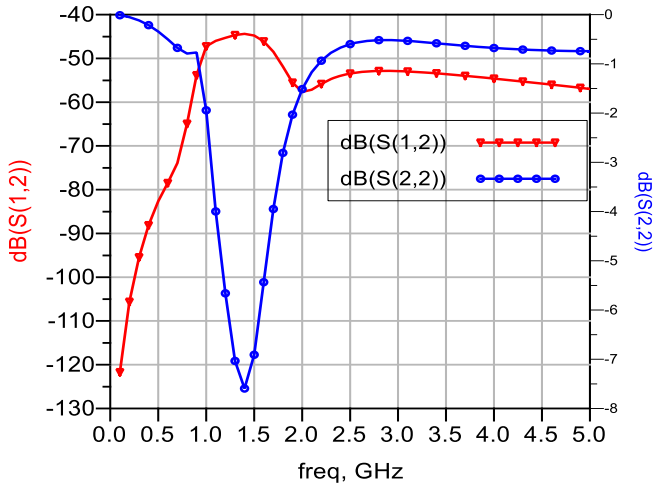

FIGURE 4.44: S_{12} and S_{22} simulation results of GPS CRLNA.

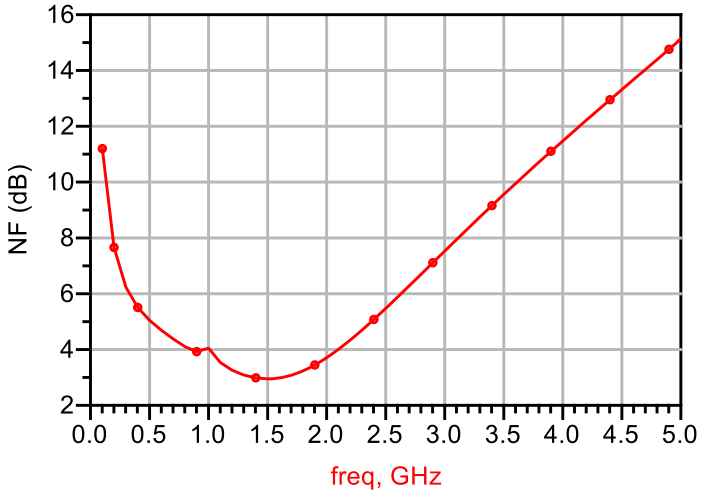

FIGURE 4.45: Noise Figure simulation results of GPS CRLNA.

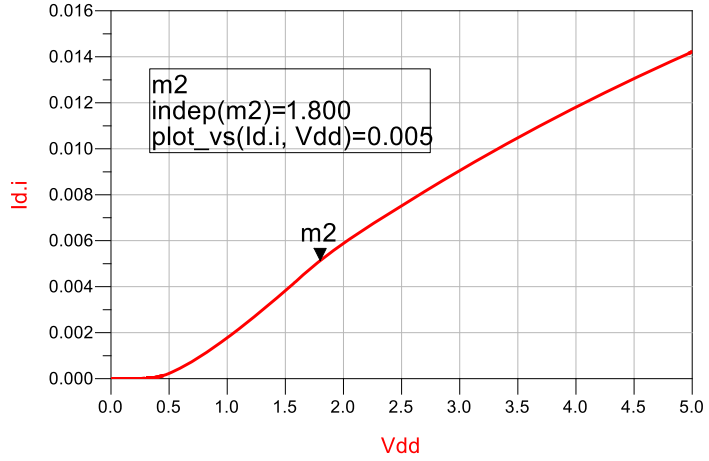

FIGURE 4.46: DC Simulation of GPS CRLNA.

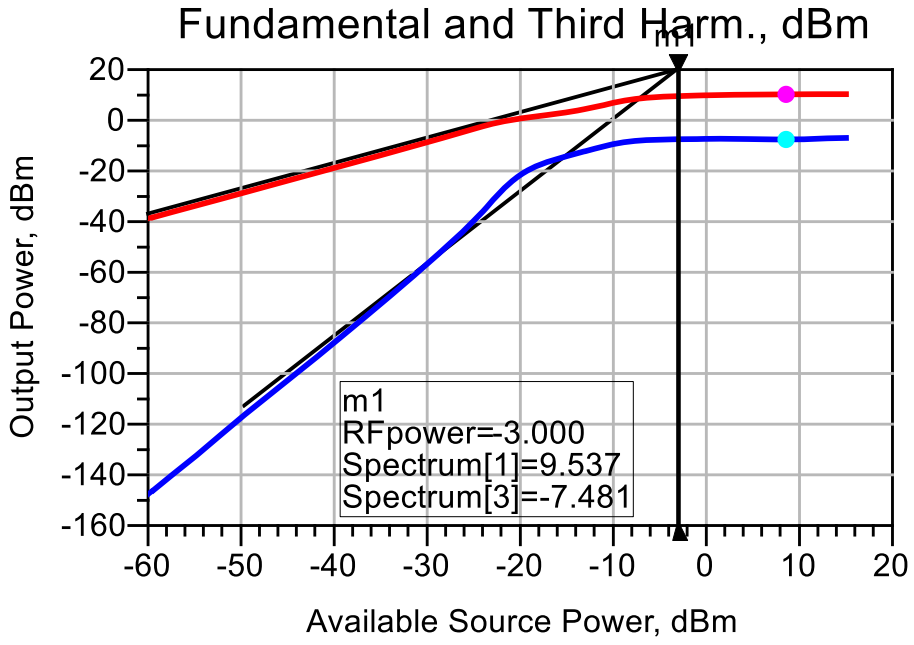

FIGURE 4.47: Harmonic simulation of GPS CRLNA.

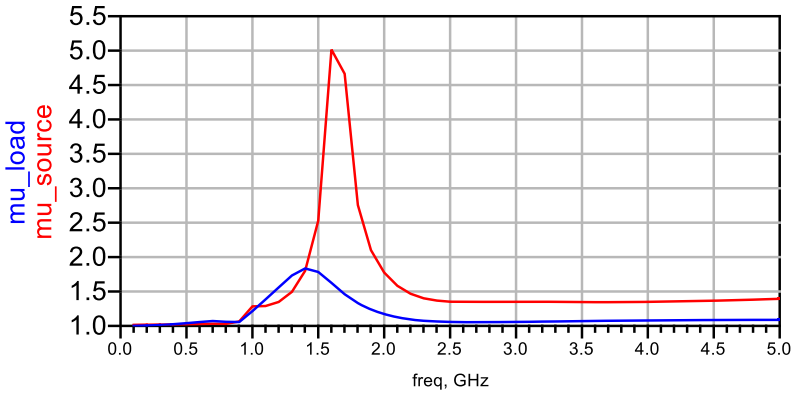

FIGURE 4.48: Stability factor simulation of CRLNA.

TABLE 4.7: GPS LNAs achieved performance comparisons with literature works.

Parameter \ Design	[85], 2009	[86], 2011	[87], 2011	Design 1 GPS IDCS LNA	Design 2 GPS CRLNA
Technology (nm)	350	180	180	180	180
Frequency (GHz)	1.575	1.575	1.575	1.575	1.575
Power Gain (dB) (S_{21})	17	10	13.7	22	24
Input matching S_{11}	-15	-15	-7.2	-25	-23
Noise Figure (dB)	1.5	3.2	2.31	3	3
Power Consuption (mW)	36	33.23	14.4	10.8	9
IIP3(dBm)	1	1.62	-5.48	1	-3
No. of Inductor	3	3	3	3	5
FOM_N	-1.03	-0.01	-3.02	6.43	3.37

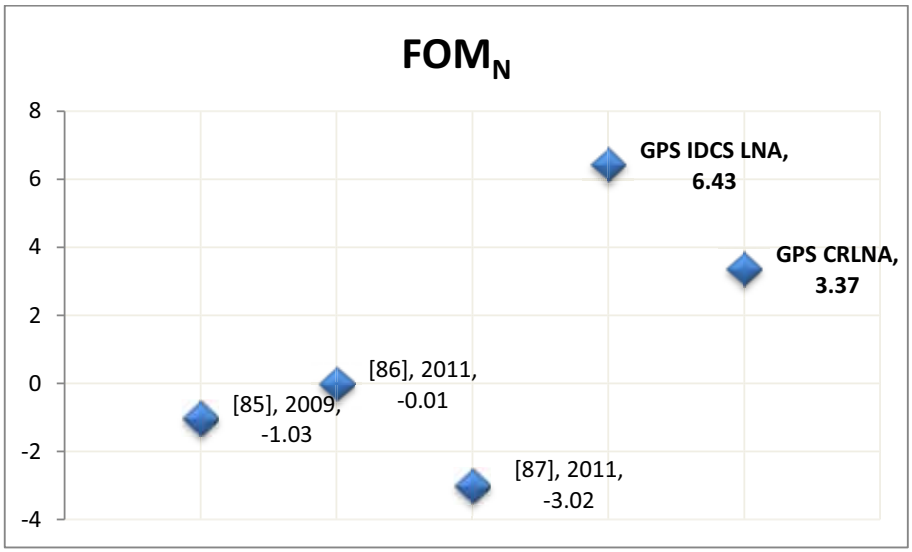

FIGURE 4.49: FOM of published and proposed GPS LNAs design.

GPS LNA using current reuse topology is designed and simulated using RFCMOS 0.18 µm technology. Simulation results of the design achieved S_{21}, S_{11}, NF, IIP3 are 25 dB, -23 dB, 3 dB and 1dBm respectively. Achieved results have very good gain, good input matching for maximum power transfer, low noise figure and good linearity. This design consumes 5 mA current from 1.8V supply as is shown in Fig. 4.46. Results of the GPS LNA designs are compared with published work as shown in the table 4.5. Stability factor is greater than one which shows the design is unconditionally stable as shown in Fig. 4.48.

CHAPTER 5

High Power Gain UWB LNA

5.1 Introduction

FCC allows use of 3.1-10.6 GHz UWB frequency spectrum, for commercial wireless communication since 2002. Due to wideband of UWB technology, opens new frontier in wireless communications and provide high data rate and less multi path fading. UWB technology is widely used in high data rate wireless communication, penetration imaging and high accuracy locating applications. Various IEEE standards adopt this technology to improve performance of wireless system.

5.1.1 Ultra Wide Band (UWB) Technology

Defense department of United State was using this technology since early 1960's, but it was not popular as UWB, but different nomenclature was used. Patent awarded to UWB communication system in 1973. Before 1980's this technology was referred as impulse, carried free, or based band communication. After 1989 this technology is popularly known as Ultra Wideband (UWB). Most of technological advance has been classified before 1994.

To utilize UWB technology for commercial wireless communication, Federal Communications Commission (FCC) has given permission with restrict to transmit low power.

5.1.2 Bandwidth and Guidelines of UWB Technology

Fig. 2.1 graphically shows the Equivalent Isotropic Radiated Power (EIRP) spectral transmission limits set by the FCC for the commercial use UWB communication. Vehicular RADAR system uses 1.61 – 3.1 GHz band. The FCC has put strict restriction on outdoor transmission limit to avoid interference with exciting system in 1.61-3.1 GHz band.

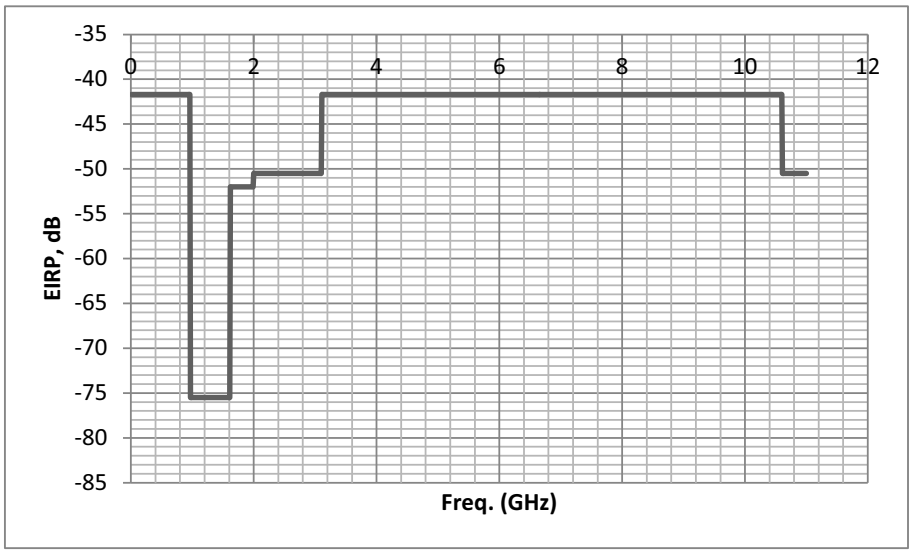

FIGURE 5.1: EIRP Emission specified by the FCC.

UWB signal is defined in terms of spectral occupancy. FCC defined UWB signal should have a spectral more than 500 MHz or more than 20% of fractional bandwidth. Fractional bandwidth is defined by the (5.1)

$$F_{bw} = \frac{Bandwidth(BW)}{Center\ Frequency} = \frac{f_{Upper} - f_{Lower}}{(f_{Upper} + f_{Lower})/2} \tag{5.1}$$

In (5.1) f_{Upper} and f_{Lower} are the upper and lower -10 dB radiation frequencies.

5.1.3 Features and Applications of UWB Technology

Extremely wide bandwidth of UWB, opens new frontier for wireless communication users. Bandwidth is the main limitation to improve performance of wireless communication. UWB have wide bandwidth, which improve communication channel capacity, quality and data rate of wireless communication. It's easily illustrating using shannon's Channel Information Capacity theorem. The shannon's theorem is state that

maximum channel capacity depend on bandwidth and signal to noise ratio as shown in (5.2).

$$C = Blog_2\left(1 + \frac{S}{N}\right) \tag{5.2}$$

Where, C is maximum theoretical capacity, B is channel bandwidth, S is signal power and N is noise power.

In narrowband system due to restricted bandwidth data rate is controlled by the transmitted power (S). UWB system has a very large channel bandwidth, which reduce need of high power transmission to establish adequate data rate. According to FCC regulations, UWB can reach data rate speed greater than 110 MB/s over 10-15 meters [88].

Due to low transmission power and high data rate in UWB technology, opens new frontier in wireless communications. UWB is widely used in high data rate short distance wireless communication, personal area networks, sensor networks, RADAR, image penetrating, medical applications and RFID. Due to low power consumption and very large bandwidth, it is used in wireless real time signal transmitting and observing of the human body [89]. Similarly various biomedical applications take advantages of UWB technology.

5.1.4 UWB System Standards

IEEE is developing several IEEE standards that adventure the UWB bandwidth specified by FCC and integrates it with the existing IEEE standards to insure good quality of service to users.

IEEE define IEEE 802.15 standard for Wireless Person Area Network (WPAN) which use UWB technology. Within this standard sub standards IEEE 802.15a is defined for high data rate communication. IEEE 802.15a is implemented using UWB system. IEEE standards improve performance by incorporate UWB technology.

5.1.5 UWB System Architectures

UWB system use two main system level approaches, Impulse type Impulse Radio UWB (IR UWB) and carrier based Orthogonal Frequency Division Multiplexing UWB (OFDM

UWB) to utilize frequency spectrum of UWB. The Multi-band OFDM Alliance supports a type of OFDM architecture referred to as Multi Band OFDM specified in www.multibandofdm.org. UWBforum propose another forum, direct sequence UWB based on IR UWB. IR UWB is included in IEEE 802.15.4a standards due to its simplicity and localization capability compared to OFDM UWB system.

Implementation of RF frontend for both the types of system architecture either IR UWB or OFDM UWB require wideband, high power gain, low noise figure and linear 3.1-10.6 GHz wideband LNA.

IMPULSE RADION UWB: IR-UWB communication use baseband pulses of very short duration as signalling and either On-Off keying (OOK), pulse-position modulation (PPM), or pulse amplitude modulation (PAM) as modulation schemes. IR UWB is used in ZigBee technology for IEEE 802.15.4 (WPAN) standard due to high date rate, low complexity and very low power.

Fig. 5.2 shows IR-UWB receiver architecture. The optimum match filter functionality is achieved using analog correlator (∫) and template generator. The optimum match filter maximized signal to noise ratio with presence of noise. At narrowband lower frequency this matched filtering function is performed using digital hardware but for RF UWB receiver to implement matched filtering in digital domain is practically impossible using current technology. ADC designing for UWB signal to operate at Nyquist rate using current technology is impossible task.

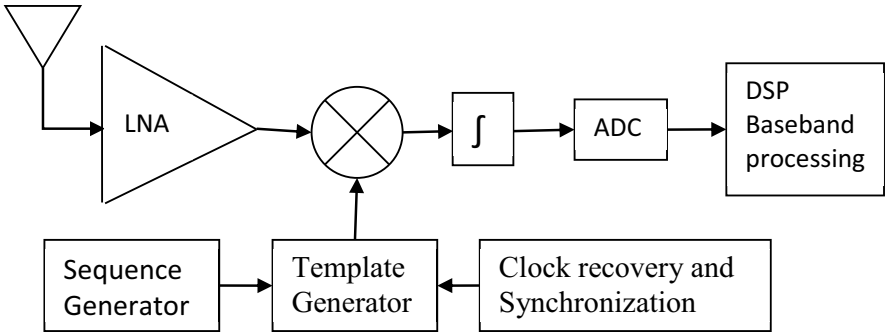

FIGURE 5.2: IR UWB Receiver architecture.

To relax ADC performance requirements, need to down convert RF signals and improve signal to noise ratio. Mixer down convert RF signals to IF band and LNA improve signal

to noise ratio of RF signals. An LNA design for an IR UWB receiver should to operate 3.1–10.6 GHz wideband with adequate power gain, input matching, low noise figure and linearity.

MULTI BAND OFDM UWB: Due to increasing demand of wireless communications recently made OFDM techniques are popular. OFDM is widely used in modern wireless communication products, to take advantage of existing design, OFDM proposed for UWB system.

The MB-OFDM systems use multiple orthogonal bands to achieve Ultra-Wideband communication as shown in Fig. 5.3.

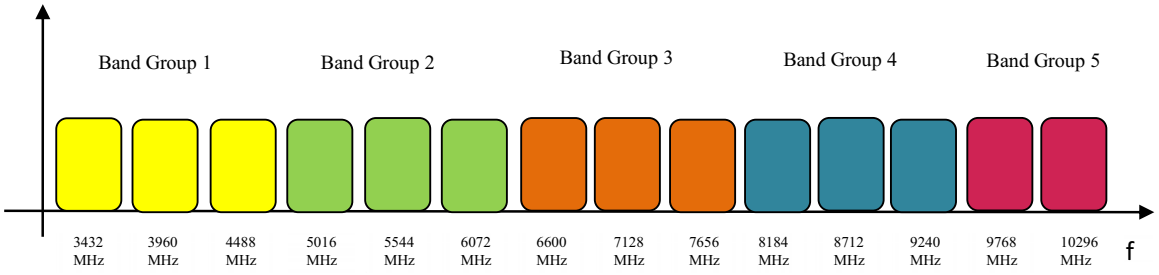

FIGURE 5.3: Multi band proposed for the IEEE 802.15.3a standard.

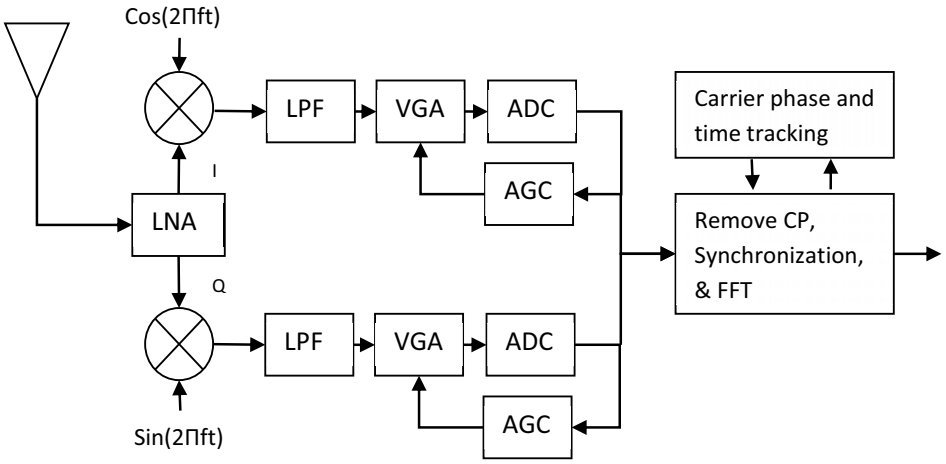

FIGURE 5.4: MB OFDM UWB receiver architecture.

Fig. 5.4 shows MB OFDM UWB receiver architecture proposed by the Multiband Alliance for IEEE 802.15.3a standards. Fig. 5.4 shows MB OFDM UWB receiver architecture is more complex compare to IR UWB receiver. The MB OFDM has higher

power consumption it makes MB OFDM not suitable for low power receiver. MB OFDM has potential to provide high data rate and it is use entire 3.1–10.6 GHz frequency spectrum of UWB.

Both the IR UWB and OFDM UWB systems achieved very high data rates but having complex receiver architecture and consuming high power.

LNA used in RF front end of UWB receiver implement using three different approaches; 1) Multiple LNAs for each band, 2) an LNA with tunable capabilities to cover entire 3.1-10.6 GHz spectrum, 3) single 3.1-10.6 GHz UWB LNA. In this thesis design 3.1-10.6 GHz UWB high power gain LNA to support both IR UWB and OFDM UWB systems.

5.2 Proposed High Power Gain UWB LNA

Proposed design for UWB LNA has CG input stage with multi cascaded CS stages. Resistive load provide wideband output matching in most of literature survey design use resistive load. Drawback of using resistance in design is adding thermal noise. In our design we have used low quality factor inductor as load. To extend bandwidth we have resonant each stage at different frequency. Our design forms cascaded three active band pass filter structure. In last stage we have used common drain to drive high capacitive load of next stage. Complete schematics of our design shown in figure this UWB LNA is design using 0.18 μm RFCMOS technology.

MULTISTAGE LNA DESIGN: The proposed UWB LNA has multi amplifier stages as shown in Fig. 5.5.

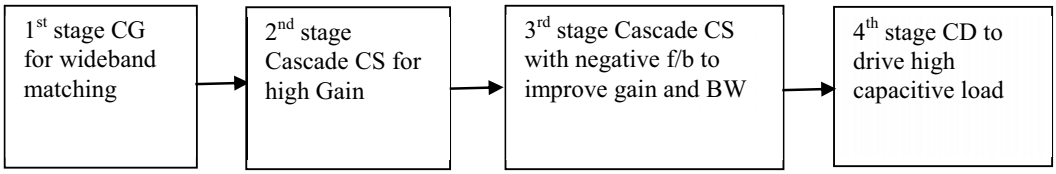

FIGURE 5.5: Different stages of proposed design.

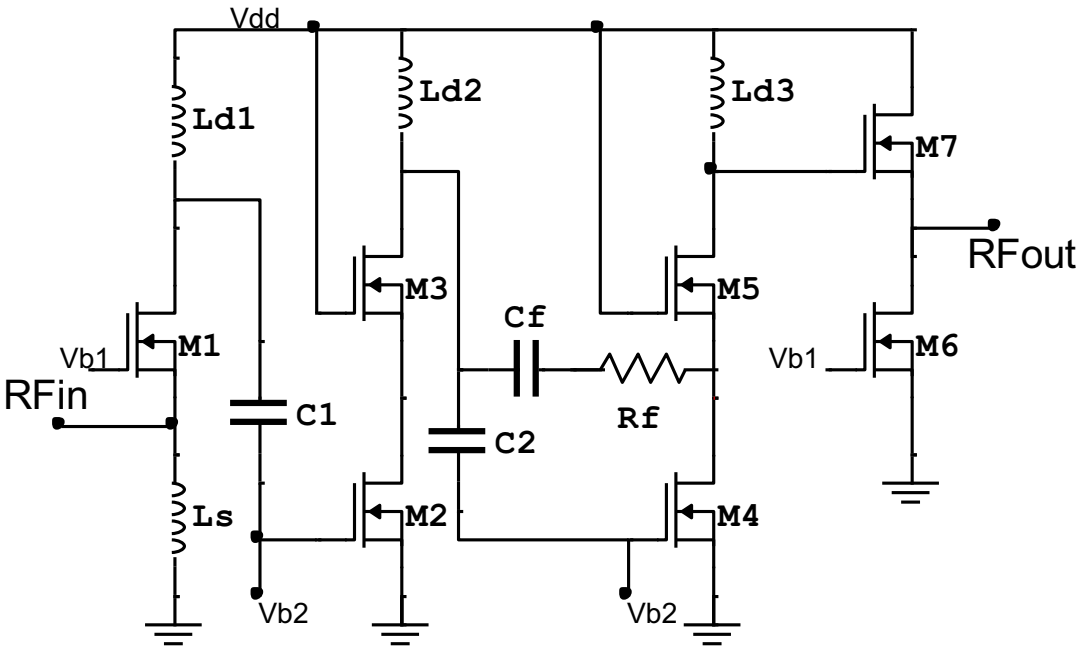

FIGURE 5.6: Ciruit diagram of proposed UWB LNA.

5.2.1 Circuit Analysis of Proposed Design

The schematic of the proposed LNA is demonstrated in Fig. 5.6. The LNA consist four stages with separate biasing circuits. The input stage of the LNA is common gate, which gives high bandwidth input matching. The inductor connected between the source of the M1 and ground provides the LC resonator with Cgs1. It also gives the input impedance matching to 50Ω. Second stage is the cascode stage to increase gain. Third stage is Cascode amplifier with series RC feedback to increase gain and bandwidth enhancement and last stage is Common Drain amplifier for drive input capacitive load for mixer [90].

In proposed LNA width of M1 is chosen to get the better transconductance with the source inductor. The large value capacitor is between the M1 gate and ground ensures better AC grounding. It is also bypasses the biasing circuit noise.

Width of M1 selection is tricky task, because value of inductor L2 restricted by the RFIC. L2 must be chosen as it will resonate with $C_{d1} + C_{gs2}$ around the center frequency of interested band. With the help of iteration the L1 value is chosen for the best noise performance. The chosen value of Ls is much greater than value of L1. Here the two LC

tank circuit formed, one is L1 with C_{gs2} + C_{gd1} and another is Ls with C_{gs1}. These both circuits resonate around the center frequency of the interested band [91].

Miller effect creates problem in the selection of the peaking frequency, to reduce miller effect the cascode transistor added to the common source stage which cause increases the higher frequency cutoff. Cascode stage also provides contribution to improve the gain and the reverse isolation, without consuming more power.

5.2.2 Input Impedance Analysis

Literature survey shows Common Gate have inherently wideband impedance matching characteristics. In this design we have used CG with inductive source (Ls) input stage for wideband matching. CG suffers from low gain in our design we have used two common source (CS) stage to improve gain and bandwidth.

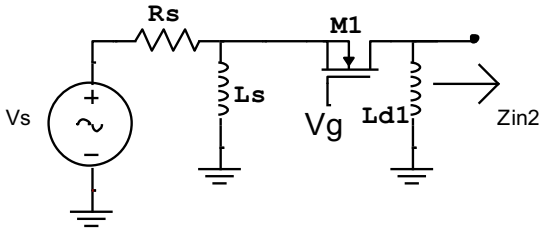

FIGURE 5.7: Common Gate input stage.

AC equivalent circuit of CG first stage is shown in Fig. 5.8.

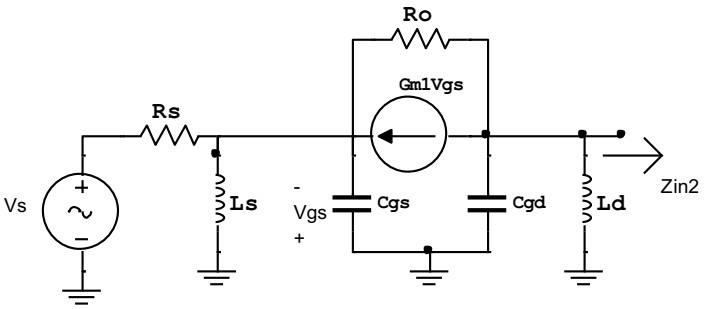

FIGURE 5.8: CG AC equivalent circuit.

The input impedance is calculated by

$$Z_{in} = \frac{-V_{gs}}{I_{in}} \tag{5.3}$$

Value of Ro is very large compared to Zo(ω). By applying KCL at input source node of MOSFET.

$$I_{in} = \frac{-V_{gs}}{Z_s(\omega)} - g_{m1}V_{gs} - \frac{(V_{gs} - g_{m1}V_{gs}Z_o(\omega))}{R_o} \quad (5.4)$$

Where, $Z_s(\omega) = j\omega L_s // \frac{1}{j\omega C_{gs}}$ and $Z_o(w) = \frac{1}{jwC_{gd}} // jwL_d // Z_{in2}$

$$Z_{in} = \frac{-V_{gs}}{I_{in}} = \frac{1}{g_{m1} + \frac{1}{Z_s(\omega)} + \frac{1 - G_{m1}Z_o(w)}{R_o}} \quad (5.5)$$

For good input matching over the wideband Ls and Cgs should be selected such that they resonate at the center frequency leaving only 50Ω real impedance.

5.2.3 Noise Analysis and Optimization

As per friss formula first stage noise figure contribute major in overall noise figure of the multistage amplifier. Noise analysis of the first common gate stage of the proposed topology is analyzed in detail.

First stage has two sources of noise, source resistor Rs and channel noise of MOSFET. Noise figure of the CG first stage can be modeled as (5.6).

$$NF1 = 1 + \frac{\overline{V_{n,d1}^2}}{\alpha^2 A_v^2} X \frac{1}{4KTR_s} \quad (5.6)$$

Where $\alpha = \frac{Z_{in}}{R_s + Z_{in}}$, $Z_{in} = SL_s // (\frac{1}{SC_{gs}})$, $\overline{V_{n,d1}^2} = \frac{4KT\gamma}{G_m}$ and $A_v = g_{m1}Z_{out}$

Substituting above values in (5.6) NF1 simplify as

$$NF1 = 1 + \frac{\gamma}{G_m}\left[\frac{(S^2L_sC_{gs1}+1)^2 R_s}{L_s} + \frac{2(S^2L_sC_{gs}+1)}{L_s} + \frac{1}{R_s}\right] \quad (5.7)$$

From the (5.7) shows first stage NF (NF1) is inversely proposal to transconductance (g_m) of M1, input and output impedance and directly proposal to C_{gs1}. NF1 can be optimized using two approaches.

- Value of L_s and C_{gs1} select such that it resonant at center of selected band.
- NF1 is inversely proposal to transconductace of the first stage (g_{m1}). Increase g_{m1} will improve NF1 but it degrades input impedance matching of the design. Here is tradeoff between input impedance and NF. Reducing C_{gs1} by reducing W of M1

will result reduction of noise figure. On the other hand, scaling down the width of means more current is consumed to maintain the same transconductance. The W_1 should be chosen such that it will improve noise performance at given power budget.

The output impendence of the source follower is calculated as

$$Z_{out}(\omega) = \frac{1+j\omega Z_3(\omega).C_{gs6}}{g_{m6}+j\omega C_{gs6}} //r_{06}//r_{07} \tag{5.8}$$

$$Z_{out}(\omega) = \frac{1+j\omega Z_3(\omega).C_{gs6}}{g_{m6}+j\omega C_{gs}6} \tag{5.9}$$

Where r_{06} and r_{07} are drain to source resistor of M6 and M7 respectively, the value these resistors are very large compare to other term so it can be neglected. Optimized design variables value of the proposed high power gain UWB LNA is given in Table 5.1.

TABLE 5.1: Components value of proposed UWB LNA design.

Components	Value	Components	Value
W_1	5.6x64 µm	Ls	1.48 nH
W_2	5.3x64 µm	Ld1	0.61 nH
W_3	5.3x64 µm	Ld2	2.10 nH
W_4	5.3x64 µm	Ld3	0.41 nH
W_5	5.3x64 µm	Vb1	0.51 V
W_6	2x20 µm	Vb2	0.62V
W_7	2x30 µm	Vdd	1.5 V
Rf	6.0 kΩ	C1	1.0 pF
Cf	120 fF	C2	1.0 pF

5.2.4 Layout of UWB LNA Design

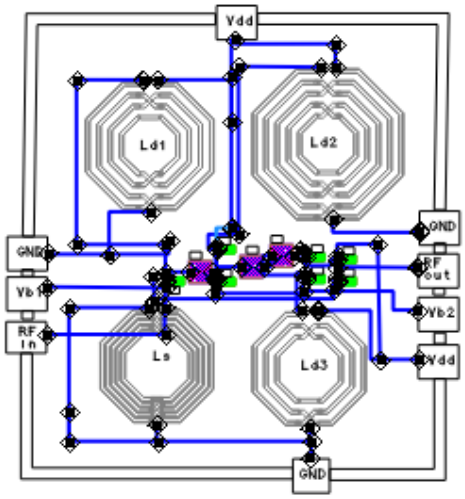

FIGURE 5.9: Layout of UWB LNA.

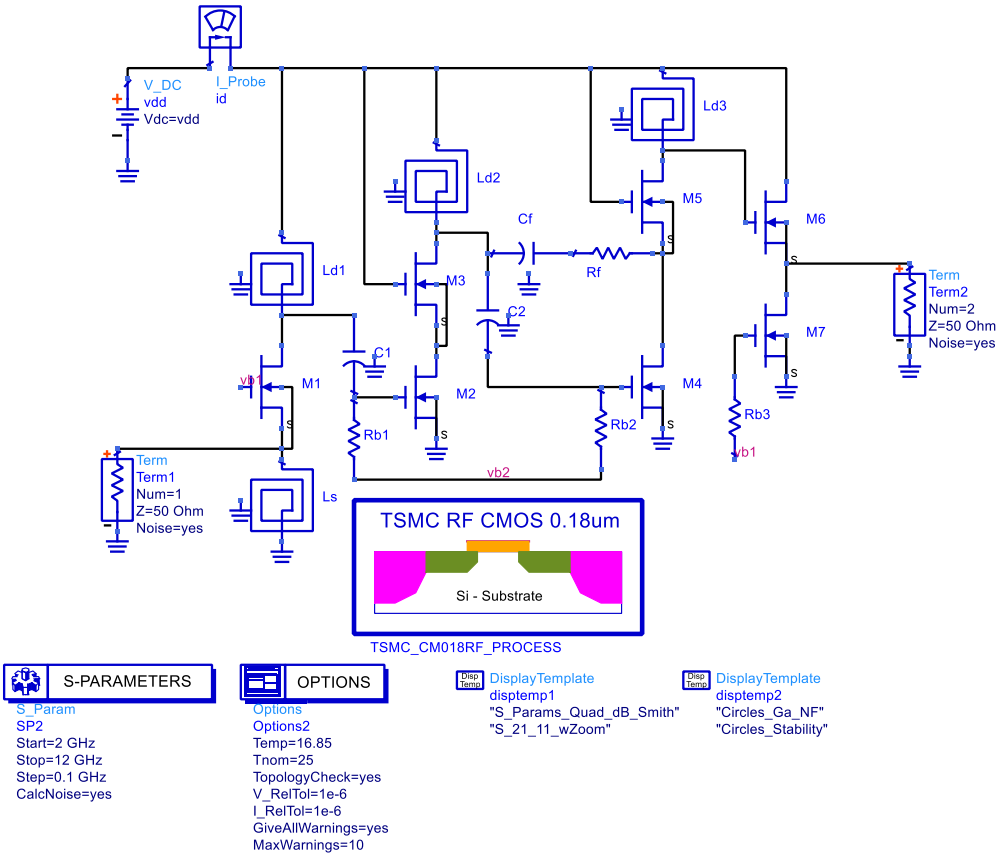

FIGURE 5.10: UWB LNA schematic

5.2.5 Simulation Results and Discussion

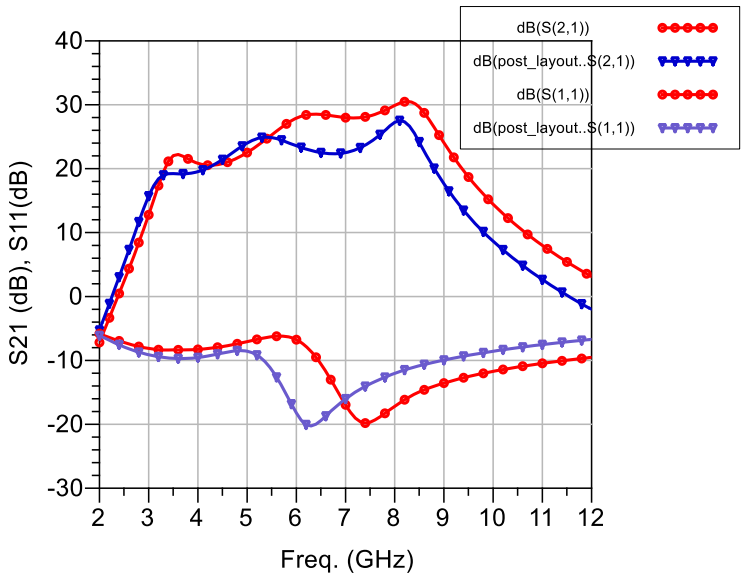

FIGURE 5.11: S_{21} and S_{11} simulation results of UWB LNA.

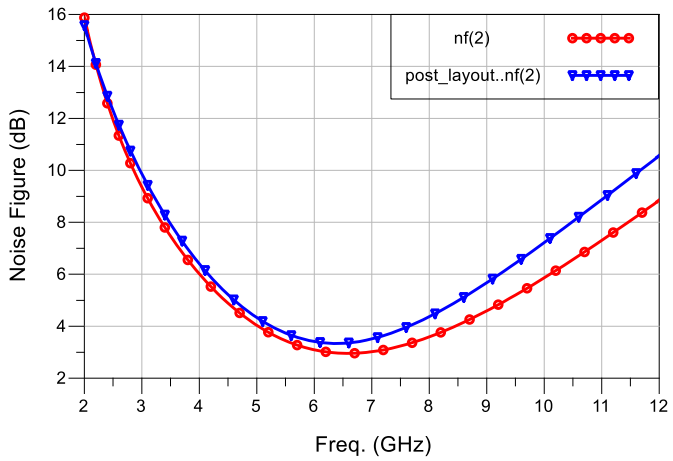

FIGURE 5.12: Noise Figure Simulation results of UWB LNA.

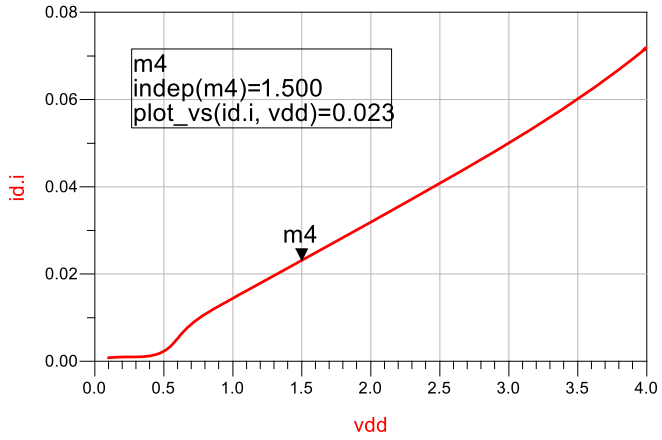

FIGURE 5.13: DC simulation result of UWB LNA.

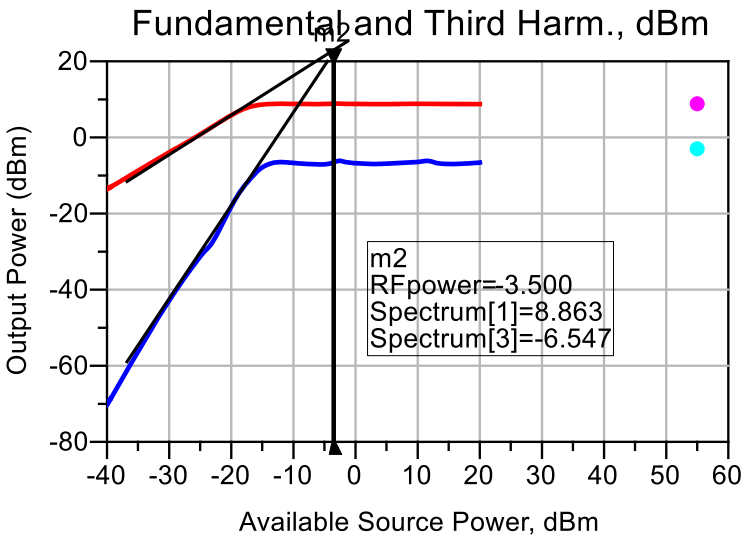

FIGURE 5.14: Harmonic simulation result of UWB LNA @ 6GHz frequency.

TABLE 5.2: IIP3 value at different frequencies of UWB LNA.

Freq.	IIP3 (dBm)
4	-13.5
5	-8
6	-3.5
7	-5
8	-3.3
9	-3

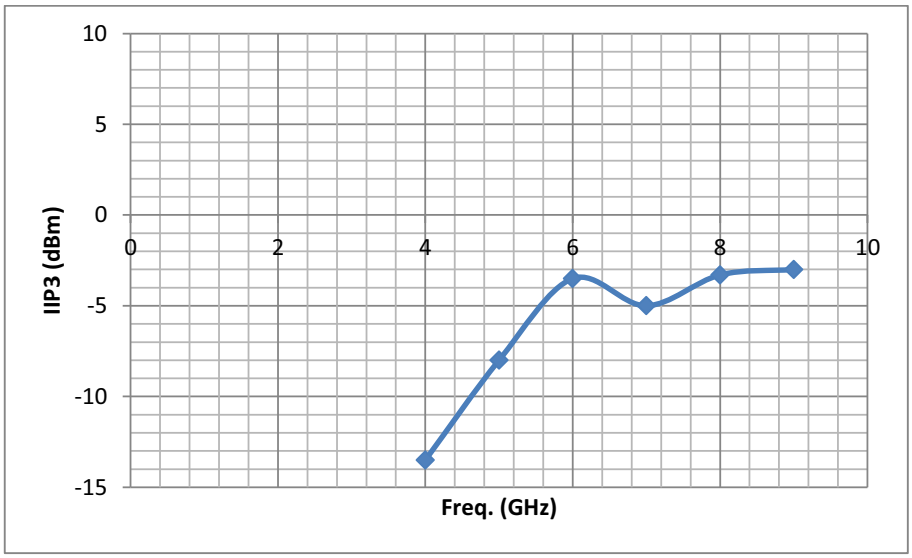

FIGURE 5.15: IIP3 versus frequency of UWB LNA.

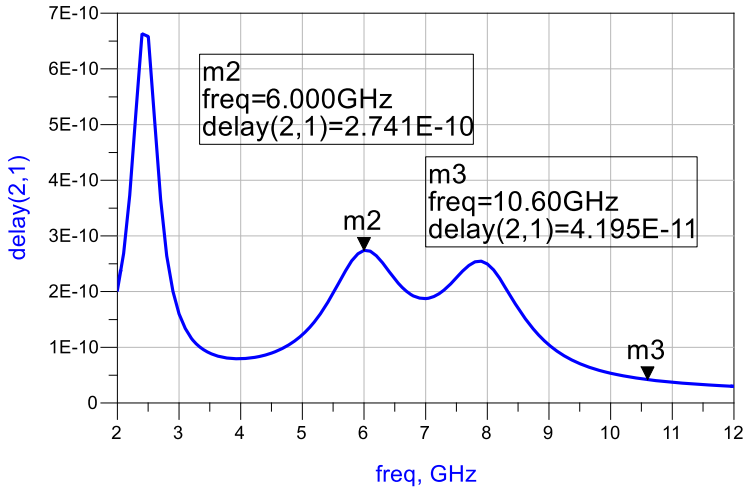

FIGURE 5.16: Group Delay variation of UWB LNA.

Simulation results of proposed UWB LNA, achieved high power gain greater than 20 dB in interested 3.1-10.6 GHz band with tolerable noise figure 2.8-6 dB. Input and output impedance matching coefficient S_{11} and S_{22} are less than -9 dB in interested band which shows good input and output matching and maximum power transfer takes place. Fig. 5.14

shows harmonic simulation of the design at 6 GHz to find linearity measure IIP3 and it achieved IIP3 is -3.5 dBm. Performed harmonic simulation at different frequencies and achieved IIP3 at different frequencies is shown in Table 5.2. Fig. 5.15 is the plot of frequency versus IIP3 of the design and it shows average IIP3 of the design is -5.5 dBm. The design is achieve good linearity by optimum biasing of each stages. DC simulation result of the design is shown in Fig. 5.13. The proposed design consuming 23 mA total current including bias circuit current from 1.5 V supply. So, total power consumption of the UWB LNA is 34 mW. Fig. 5.16 is the group delay simulation result of the UWB LNA. Group delay variation of the proposed UWB LNA is ±100ps.

Compare proposed design results with published work is given in Table 5.3. It is observed from Table 5.3 that the proposed UWB LNA design having very high power gain, good linearity and wideband impedance matching with tolerable noise figure. Due to high power gain our design is most suitable for low power signal UWB receiver RFIC and it will open new frontier for UWB wireless communication receiver design. Figure 5.17 shows FOM comparison of the proposed UWB LNA design with published UWB LNA design. Proposed UWB LNA design achieved 32.99 FOM.

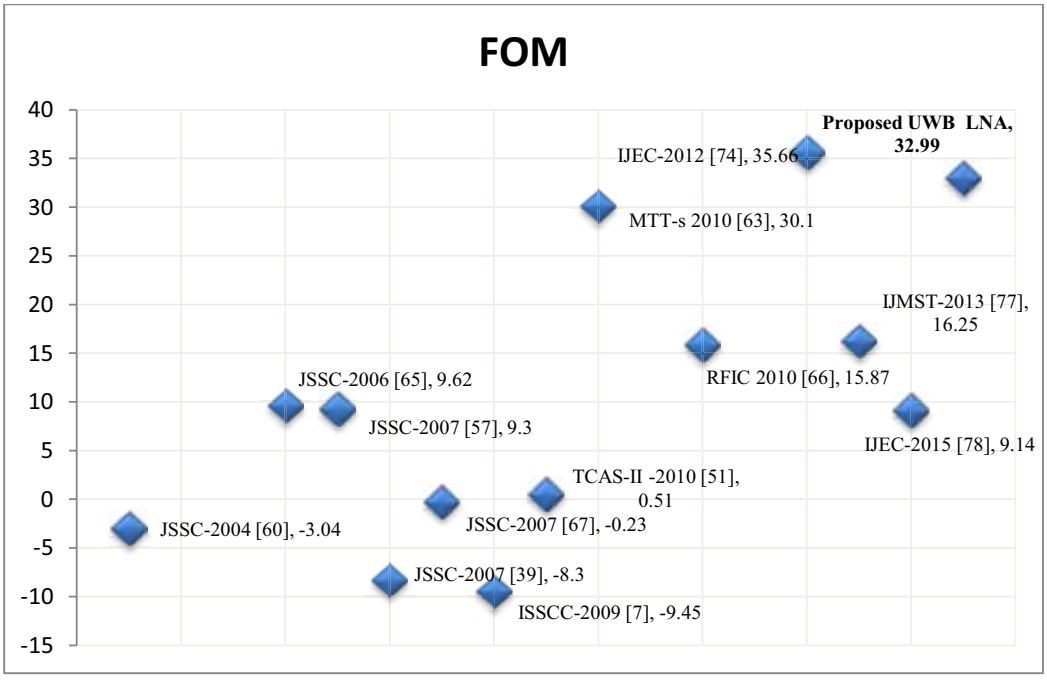

FIGURE 5.17: FOM Comparison of Proposed UWB LNA with published work.

TABLE 5.3: Comparison of achieved results with published Wideband Low Noise Amplifier.

Parameter / Source	CMOS Technology (um)	Freq. (GHz)	S_{21} (dB)	S_{11} (dB)	NF (dB)	IIP3 (dBm)	Power Consumption (mW)	Area (mm^2)	LNA Topology	FOM
JSSC-2004 [60]	0.18	2.3-9.2	9.3	<-10	4	-6.7	9	0.66	CS + degeneration and input BPF	-3.04
ICAT-2005 [62]	0.18	2.7-9.3	10	<-10	3.3	-0.3	14	-	Cascode + input HPF	-
JSSE-2006 [64]	0.18	3.1-10.6	9.5	<-8.6	5-5.6	-13	9.4	-	Cascode + input filter	-
JSSC-2006 [65]	0.18	0.04-7	8.6	<-16	4.2	+3	9	1.16	Distributed cascode	9.62
JSSC-2007 [57]	0.13	3.1-10.6	15.1	<-9.9	2.5	-8.5	9	0.87	CS + reactive FB	9.3
JSSC-2007 [39]	0.18	1.2-11.9	9.7	<-11	4.7	-6.2	20	0.59	CG + noise cancellation	-8.3
JSSC-2007 [67]	0.18 SiGe	0.1-11	8	<-12	2.9	-3.55	21.6	0.76	Distributed	-0.23
ISSCC-2009 [7]	0.13	3.1-10.6	15	-12	<4.5	-12.5	26	0.435	Weighted Distributed Cascode	-9.45
TCAS-II - 2010 [51]	0.18	3.1-10.6	13.9	<-9.4	4.7	-8.5	14.4	0.46	Parallel RC FB	0.51
MTT-s 2010 [63]	0.09	3.1-10.6	10.5	-10	3.2	4	21.6	0.139	Cs + Π input filter	30.1
MTT-S 2010 [70]	0.18	31.-10.6	13	-8.6	4.68	-12	10.34	-	CS + RLC input filter	-
RFIC 2010 [66]	0.09	21	15.4	-	6	-6.6	12.5	0.41	Distributed CS with tapered transmission line	15.87
IET MAP 2012 [72]	0.18	2.4-11.2	14.8	-	3.9	-11.5	3.4	-	CG + current reuse	-
IJEC-2012 [74]	0.18	3.1-10.6	15	<-11	3.5-3.9	6.4	16.2	0.39	Inverter with FB	35.66
IJMST-2013 [77]	0.18	2.5-16	11	<-7	3.3	-5	20	0.18	RC FB CS + current reuse	16.25
IJEC-2015 [78]	0.13	2.35-9.37	10.3	<-8	3.68	-4	9.97	0.39	CG current resue + noise cancelling	9.14
High power gain UWB LNA	**0.18**	**3.1-10.6**	**20-30**	**<-9**	**2.8-6**	**-5.5**	**34**	**0.176**	**CG+Cascode CS**	**32.99**

CHAPTER 6

Multi Standard Wideband LNAs

6.1 Introduction

To support 4G standards LTE, WiMAX with existing 2G and 3G standards GSM, CDMA, Bluetooth, Zigbee, RFID, wireless LAN (802.11a/b/g) etc. wireless standards require 0.6-5.6 GHz wideband high performance receiver. Table 6.1 shows required receiver specifications of the different wireless standards. The multi standard universal receiver requires wideband matching, high gain, high linearity and low noise figure Low Noise Amplifier (LNA). The design of low power wideband LNA for multi standards receiver using current technology is still a challenging task.

TABLE 6.1: Sensitivity, Linearity and Noise Figure specifications of different standards.

	WCDMA	WLAN	WiMAX	Bluetooth	GSM/PCS	LTE	RFID
P_{sens} (dBm)	-117	-65	-65	-70	-102	-102	-70
SNR (dB)	5.2	28	24	21	9	8	11.6
NF (dB)	9	7.5	7	23	9	9	39
IIP3 (dBm)	-4	-20	-8	-15	-18	-7	-20

Various wideband LNA are proposed in literature using different wideband LNA topologies. This chapter, propose and design two wideband LNAs. The first LNA design is proposed for highly linear multi standards universal receiver and the second LNA design is proposed for high power gain multi standards universal receiver.

NMOS/PMOS inverter structure is widely used in highly linear low power dissipation LNA design. Due to complementary characteristics of NMOS and PMOS transistors, NMOS/PMOS inverter structure cancel the distortion and improve linearity of the design. Sharing the bias current by the NMOS and PMOS transistors in inverter structure it reduces power dissipation. The proposed highly linear multi standard wideband LNA design is based on NMOS/PMOS inverter current reuse amplifier structure.

6.2 NMOS/PMOS Inverter Structure Amplifier

The complementary characteristic of NMOS and PMOS transistors is used in NMOS/PMOS inverter to enhance the linearity of the LNA.

An inverter structure is a basic common source amplifier gain stage. Compared to a CS stage an inverter has a lower NF with the same DC current. This is due to the current reuse technique or gm enhance as it is called. Total transconductance of inverter is summation of transconductances of NMOS and PMOS. Transconductance to current ratio of the NMOS/PMOS inverter structure is expressed as shown in (6.1).

$$\frac{g_m}{I} = \frac{g_{m,n}}{I_D}\left(1 + \frac{g_{m,p}}{g_{m,n}}\right) \approx \frac{g_{m,n}}{I_D}\left(1 + \sqrt{\frac{K_P W_P}{K_N W_N}}\right) = \frac{g_{m,n}}{I_D}\xi \qquad (6.1)$$

Where, ξ is the inverter efficiency factor and it can be seen that for fixed $g_{m,n}/I_D$ and W_n the efficiency is greater than one. When Wp = WnKn/Kp the efficiency factor ξ is equal to 2 meaning that the g_m is twice for an inverter than CS stage.

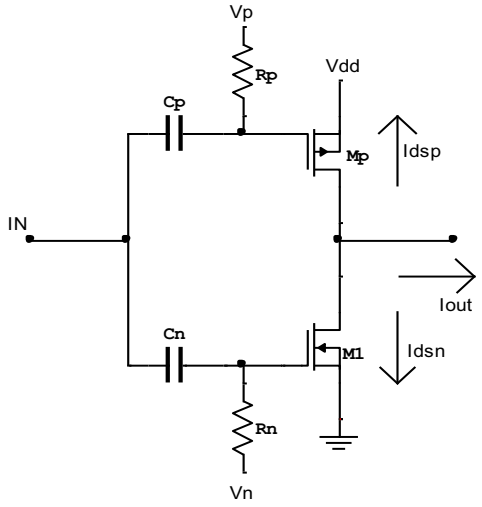

FIGURE 6.1: NMOS/PMOS inverter structure.

A drawback of NMOS/PMOS inverter structure is the higher input capacitance. Total input capacitance of inverter structure is addition of NMOS and PMOS gate to source capacitance.

$$C_{IN} = C_{gs,n} + C_{gs,p} = C_{gs,n}\left(1 + \frac{W_p}{W_n}\right) \tag{6.2}$$

Input capacitance of inverter is higher by the factor of (1+Wp/Wn) compared to the input capacitance of a CS stage of

$$C_{IN} = C_{gs,n} \tag{6.3}$$

When both the transistors are biased in saturation region inverter structure LNA achieve maximum gain. The small signal voltage gain of inverter structure can be expressed as:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-(g_{mn}+g_{mp})}{g_{dsn}+g_{dsp}} \tag{6.4}$$

6.2.1 Linearity Analysis

Fig. 6.1 shows the NMOS/PMOS inverter configuration amplifier. In Inverter structure input is applied at tied gate of both NMOS and PMOS transistors and output from short circuited drain of both transistors. Due to nonlinearity of the MOSFET output drain current of NMOS and PMOS can be expressed as follows:

$$I_{dsn} = g_{1A}V_{gs} + g_{2A}V_{gs}^2 + g_{3A}V_{gs}^3 + \cdots \tag{6.5}$$

$$I_{dsp} = -g_{1B}V_{gs} + g_{2B}V_{gs}^2 - g_{3B}V_{gs}^3 + \cdots \tag{6.6}$$

$$I_{out} = I_{dsn} - I_{dsp} = (g_{1A} + g_{1B})V_{gs} + (g_{2A} - g_{2B})V_{gs}^2 + (g_{3A} + g_{3B})V_{gs}^3 \tag{6.7}$$

Where, g_1, g_2 and g_3 are the main transconductance, second-order and third-order nonlinearity coefficients respectively. The second order nonlinearity is cancelled in output due to out off phase signals of NMOS and PMOS transistors. The linearity measure IIP3 is inversely propos anal to third order nonlinearity coefficient. The optimum biasing reduce g3, hence improve linearity of the design.

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|} \tag{6.8}$$

Inverter structure has two gain devices, NMOS and PMOS to boost overall transconductance. With the proposed technique, reducing g3 and increasing g1 leads to highly linear and high gain performance over a wide range of frequencies.

6.3 Resistive Feedback Inverter Wideband LNA

The CS resistive shunt feedback is the most popular wideband design technique due to its simple design and superior broadband characteristics. The resistive feedback CMOS inverter wideband LNA topology is shown in Fig. 6.2. Using resistive feedback in inverter achieve wideband input matching. The second stage in this design is a CS cascode to improve gain and isolation.

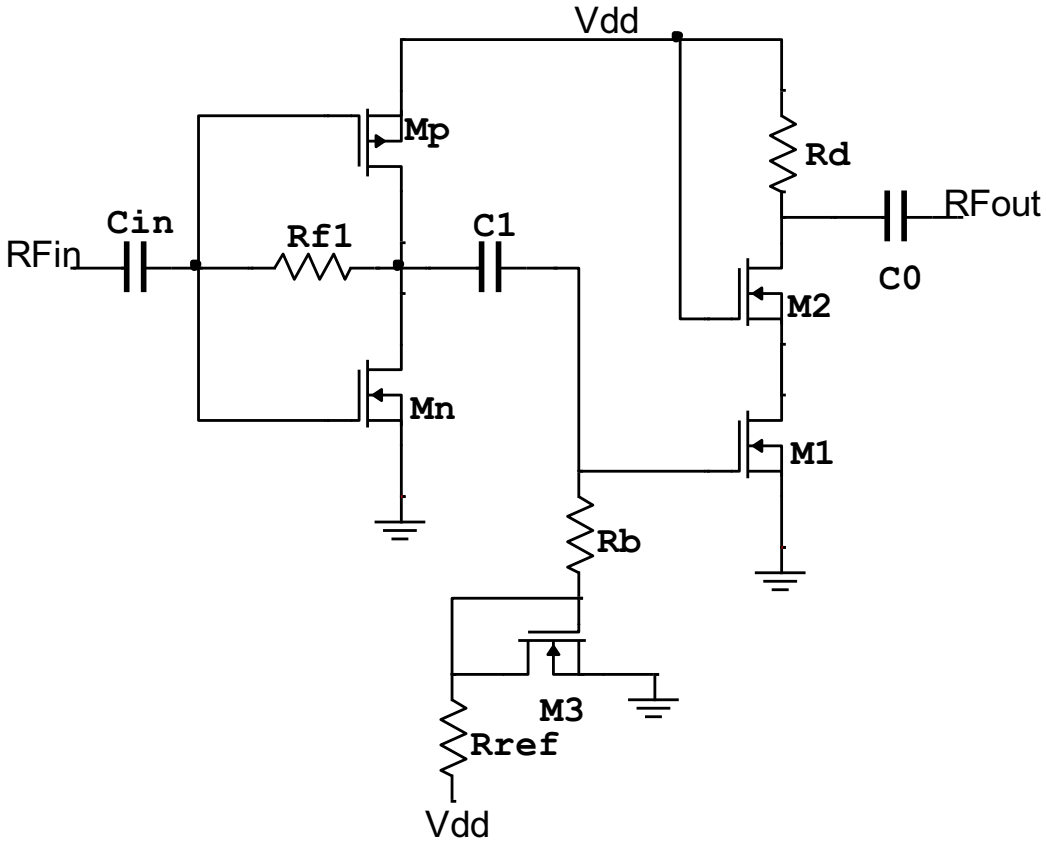

FIGURE 6.2: Resistive feedback inverter wideband LNA schematic.

6.3.1 Input Impedance Analysis

Input impedance of current reuse inverter NMOS/PMOS with resistive feedback derived is similar to CS with resistive feedback discuss in literature chapter. Transconductance of inverter is $g_m=g_{mn}+g_{mp}$.

Input impedance of the resistive feedback inverter structure with cascode CS next stage is expressed as

$$Z_{in} = \frac{R_F+Z_{in2}}{1+(g_{mn}+g_{mp})Z_{in2}} \tag{6.9}$$

Where, Z_{in2} is the input impedance of cascode CS next stage.

$$Z_{in2} = \frac{1}{SC_{gs2}} \tag{6.10}$$

At lower frequency Z_{in2} is very large and it can be neglected. So, input impedance of first stage at lower frequency is simplified as

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_m} \tag{6.11}$$

At higher frequency value of Z_{in2} is comparable to R_F, and Z_{in} is

$$Z_{in} = \frac{R_F+\frac{1}{SC_{gs2}}}{1+g_m\frac{1}{SC_{gs2}}} = \frac{R_FSC_{gs2}+1}{SC_{gs2}+g_m} \tag{6.12}$$

Equation (6.12) shows Z_{in} is directly proposal to R_F and inversely proposnal to g_m.

6.3.2 Voltage Gain and Noise Figure Analysis

Similarly to CS amplifier voltage gain of CMOS inverter with resistive feedback is expressed as

$$A_v = \frac{V_{out}}{V_{in}} = 1-(g_{mn}+g_{mp})R_f \tag{6.13}$$

Noise figure of NMOS/PMOS inverter structure can be found same as resistive feedback CS amplifier is derived in literature chapter. NF of the resistive feedback is expressed as

$$NF = 1 + \frac{R_S}{R_F}\left(1 + \frac{1}{(g_{mn}+g_{mp})R_S}\right)^2 + \frac{\gamma}{(g_{mn}+g_{mp})R_S} \quad (6.14)$$

Equation (6.14) shows Noise figure of the resistive feedback inverter wideband LNA is inversely proposnal on feedback resistance R_F. Higher value of feedback resistor minimize noise figure but it degrades input impedance matching. Selection of feedback resistance value has tradeoff between to achieve wideband impedance matching and low noise figure of design. Bandwidth of resistive feedback is expressed using (6.15).

$$BW = \frac{1+A_v}{R_F(C_{gs}+(1+A_v)C_{gd})} \quad (6.15)$$

Where, Av is the open loop gain, R_F is the feedback resistor, and C_{gs} and C_{gd} are the parasitic capacitors of the MOSFET.

TABLE 6.2: Components value of resistive feedback inverter LNA.

Components	Value	Components	Value
W_n	6.3x30 µm	Rf	330 Ω
W_p	6.3x30 µm	Rd	50 Ω
W_1	4.6x64 µm	Cin, C1, Co	3 pF
W_2	4.6x64 µm	Vdd	1.2 V
W_3	1.5x30 µm	Rb, Rref	2 KΩ

6.3.3 Simulation Results and Discussion

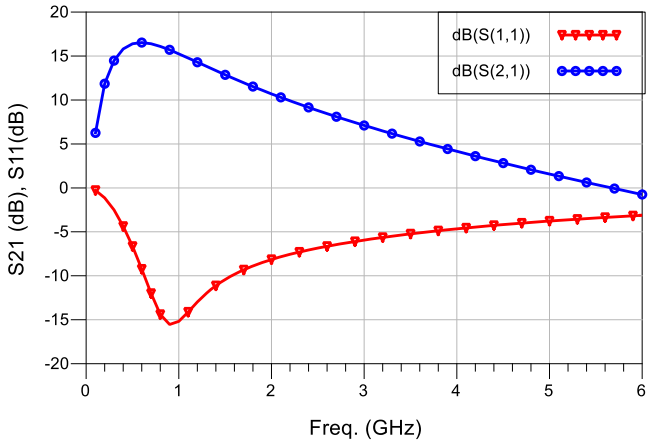

FIGURE 6.3: S_{21} and S_{11} simulation results of resistive feedback inverter LNA.

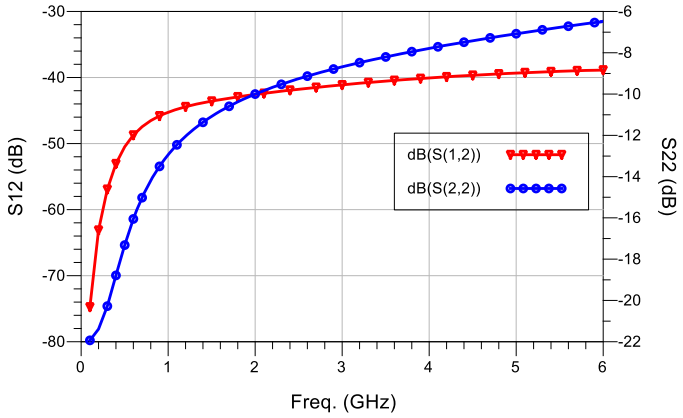

FIGURE 6.4: S_{12} and S_{22} simulation results of resistive feedback inverter LNA.

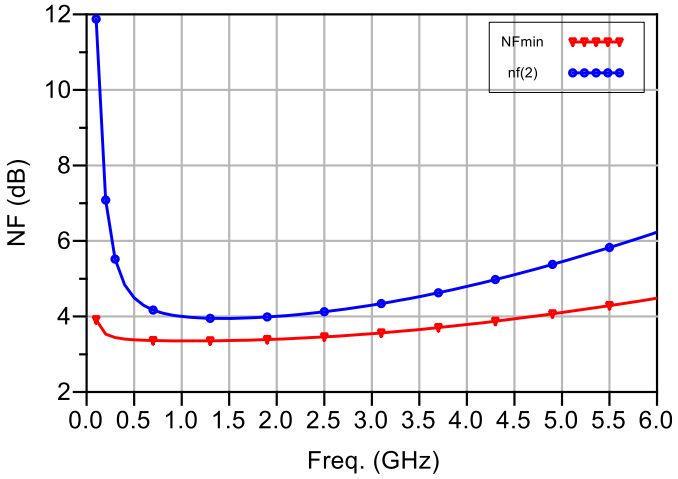

FIGURE 6.5: Noise Figure simulation results of resistive feedback inverter LNA.

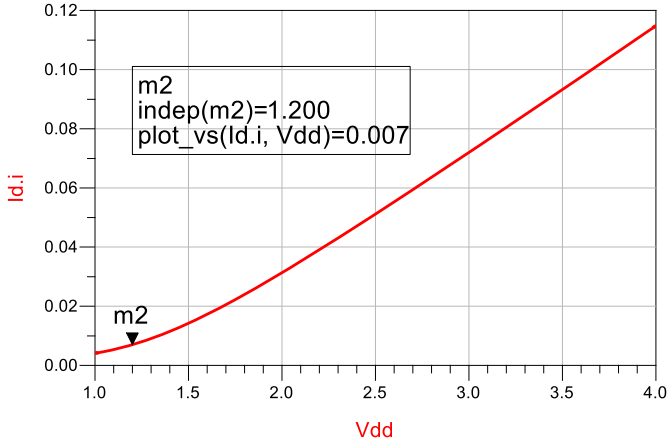

FIGURE 6.6: DC simulation result of resistive feedback inverter LNA.

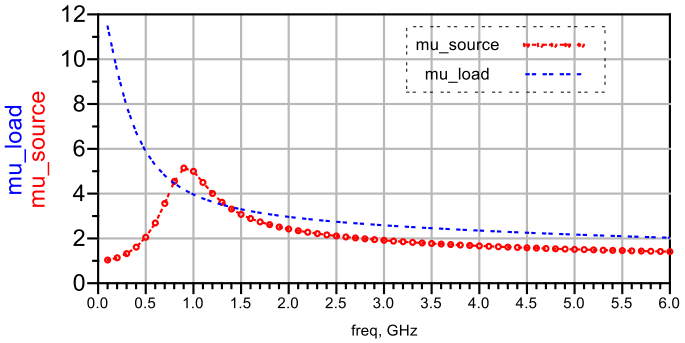

FIGURE 6.7: Stability simulation result of resistive feedback inverter LNA.

The resistive feedback inverter wideband LNA is designed using TSMC 0.18 µm RFCMOS MOSFET model and the design is simulated using ADS RF circuit simulator. Simulation results of S_{21} and S_{11} shows gain decreasing and input matching degrading at higher frequency as shown in Fig. 6.3 this is due to higher input capacitance of inverter structure. At lower frequency reactance of input capacitance is very high which make pure resistive input impedance and provide good matching. Simulation results shows the design has well <4 dB NF, <-40 dB S_{12}, <-8 dB S_{22} in interested 0.6-5.6 GHz wideband. DC simulation result show the design is consuming only 7 mA total current including bias circuit from 1.2 V supply.

At higher frequency reactance of input capacitor is decreasing and makes capacitive impedance which degrades input matching at higher frequency and also decreases gain. To nullify capacitive effect need pole in input impedance function that can be add by putting series inductor with gate of NMOS. Schematic of the resistive feedback inverter with gate inductor wideband LNA is shown in Fig. 6.8.

6.4 Resistive Feedback Inverter with Gate Inductor Lg Wideband LNA

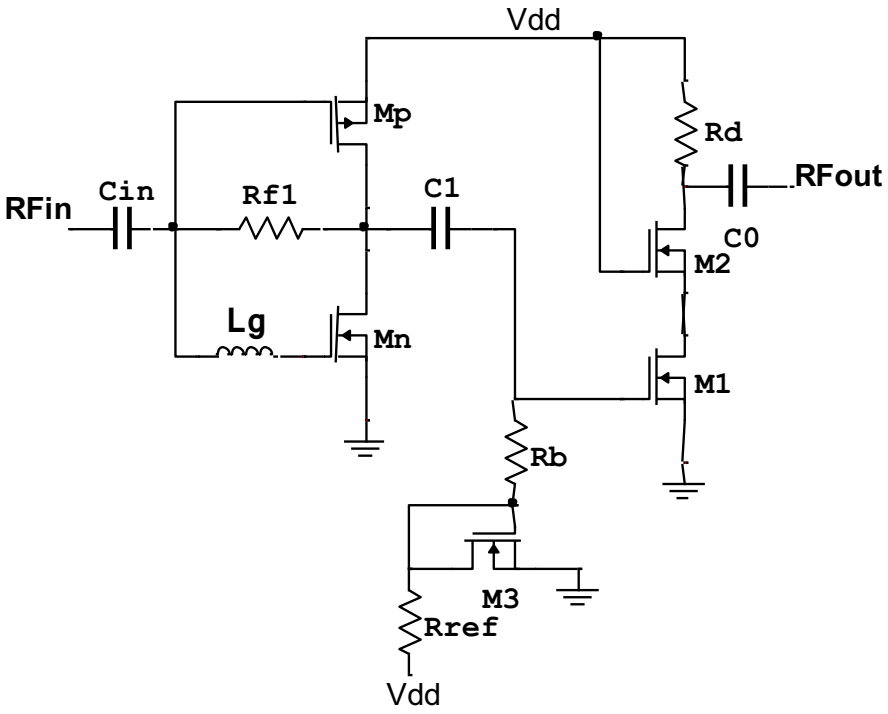

FIGURE 6.8: Resistive feedback inverter with gate inductor wideband LNA.

6.4.1 Circuit Analysis

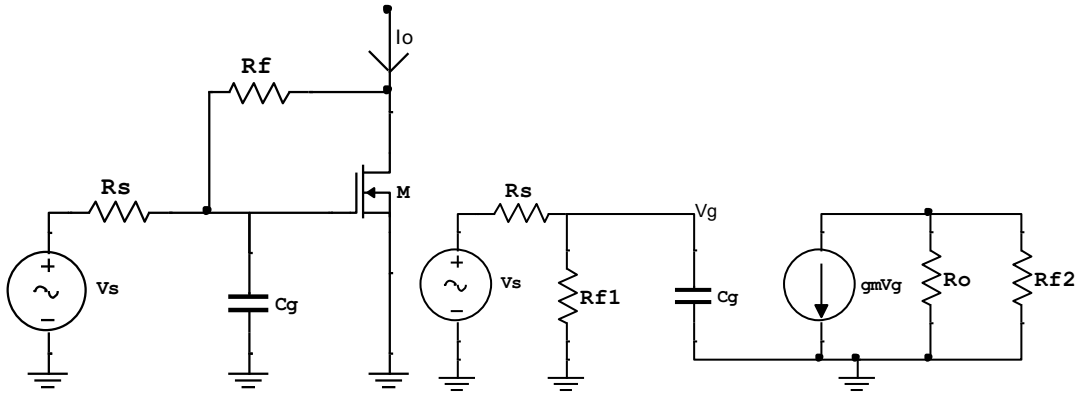

FIGURE 6.9: Resistive feedback inverter and its AC equivalent circuit.

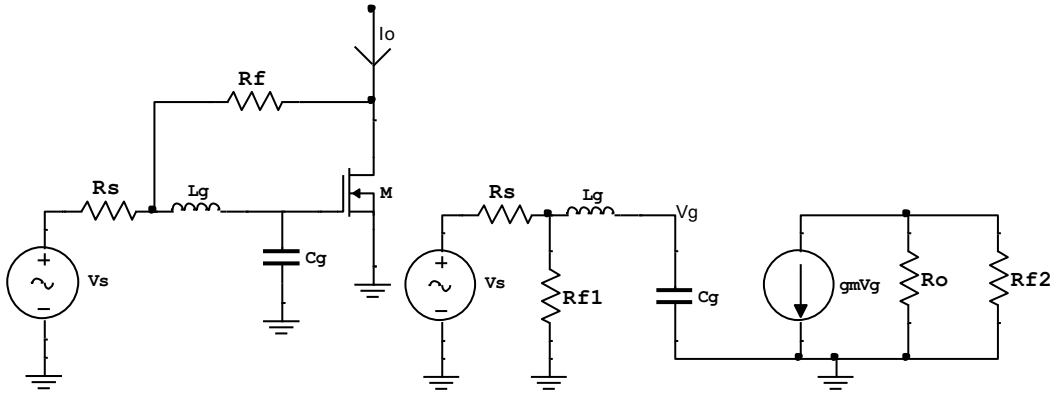

FiGURE 6.10: Resistive feedback inverter with gate inductor and its AC equivalent circuits .

AC equivalent circuit of resistive feedback inverter amplifier is shown in Fig. 6.10 where, R_{f1} and R_{f2} are miller equivalent resistors of R_f and C_g is the sum of C_{gsn}, C_{gsp} and Miller equivalent capacitance of C_{dsn}+C_{dsp}. Gate voltage of MOSFET in terms of source voltage is derive using voltage divider rule and it expressed as

$$v_g = v_s \frac{R_{f1}\left\|\frac{1}{sC_g}\right.}{R_s+R_{f1}\left\|\frac{1}{sC_g}\right.} = v_s \frac{R_{f1}}{R_s R_{f1} C_g s+(R_s+R_{f1})} \tag{6.16}$$

From the Fig. 6.9 and (6.16) voltage gain of resistive feedback inverter amplifier is express as

$$A_v = -\frac{g_{m1} v_g (R_{f2}\|r_{01})}{v_s} = \frac{g_{m1} R_{f1} (R_{f2}\|r_{01})}{R_s R_{f1} C_g s+(R_s+R_{f1})} \tag{6.17}$$

Equation 6.17 shows voltage gain transfer function has one pole at

$$s = -(R_s + R_{f1})/R_s R_{f1} C_g \tag{6.18}$$

Inverter structure with gate inductor schematic and its AC equivalent circuit is shown in Fig. 6.10. By taking

$$X_g = sL_g + \frac{1}{sC_g} \tag{6.19}$$

From the Fig. 6.10 gate terminal voltage of resistive feedback inverter with gate inductor expressed as

$$v_g = v_s \frac{R_{f1}\|X_g}{R_s+R_{f1}\|X_g} \frac{\frac{1}{sC_g}}{X_g} \tag{6.20}$$

Voltage gain of resistive feedback inverter with gate inductor is derived as

$$A_v = -\frac{g_{m1} v_g (R_{f2} \| r_{01})}{v_s} \tag{6.21}$$

$$= \frac{g_{m1} R_{f1} (R_{f2} \| r_{01})}{(R_s + R_{f1}) L_g C_g} \frac{1}{S^2 + \frac{\omega_o}{Q_o} s + \omega_o^2} \tag{6.22}$$

Where,

$$\omega_o = \frac{1}{\sqrt{L_g C_g}} \tag{6.23}$$

$$Q_o = \frac{\sqrt{L_g C_g}(R_s + R_{f1})}{R_s R_{f1} C_g} \tag{6.24}$$

Higher cut off frequency of the resisitive feedback with gate inductor design is increased by pushing pole at higher frequency using gate inductor value. The pole splitting mechanism is shown in Fig. 6.11. Value of the output quality factor depend on gate inductor as shown in (6.24). Amplifier having higher Q will produce gain peaking and lower quality factor gives better gain flatness.

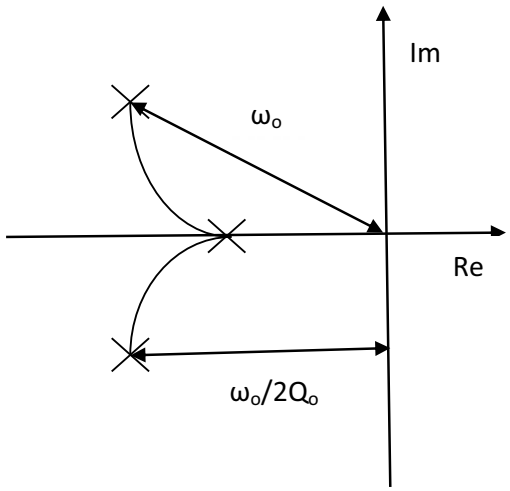

FIGURE 6.11: Pole spiliting in S plane.

TABLE 6.3: Components value of resistive feedback with Lg inverter LNA design.

Component	Value	Component	Value
W_n	6.3x30 µm	Rf	330 Ω
W_p	6.3x30 µm	Rd	50 Ω
W_1	4.6x64 µm	Cin, C1, Co	3.0 pF
W_2	4.6x64 µm	Vdd	1.2 V
W_3	1.5x30 µm	Rb	2.0 KΩ
Rref	1.0 KΩ	Lg	1.36 nH

6.4.2 Simulation Results and Discussion

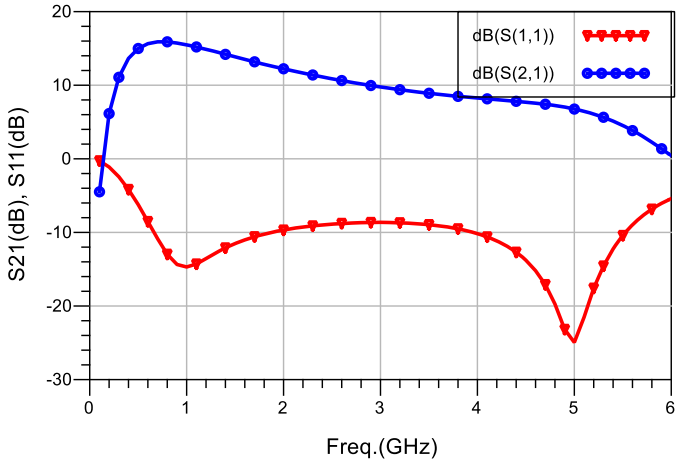

FIGURE 6.12: S_{21} and S_{11} simulation results of resistive feedback inverter with Lg LNA.

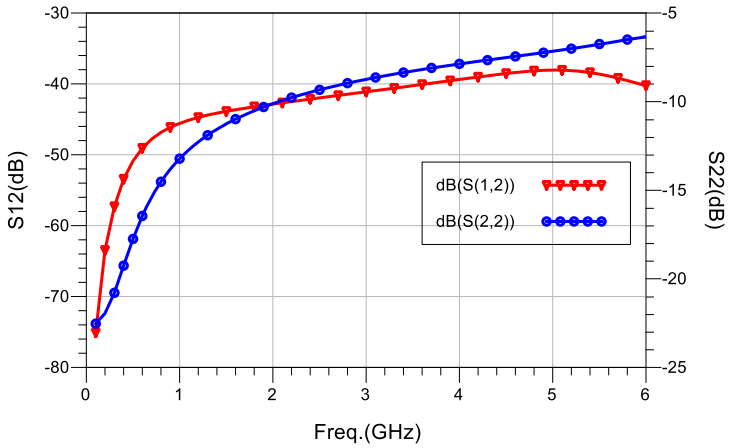

FIGURE 6.13: S_{12} and S_{22} simulation results of resistive feedback inverter with Lg LNA.

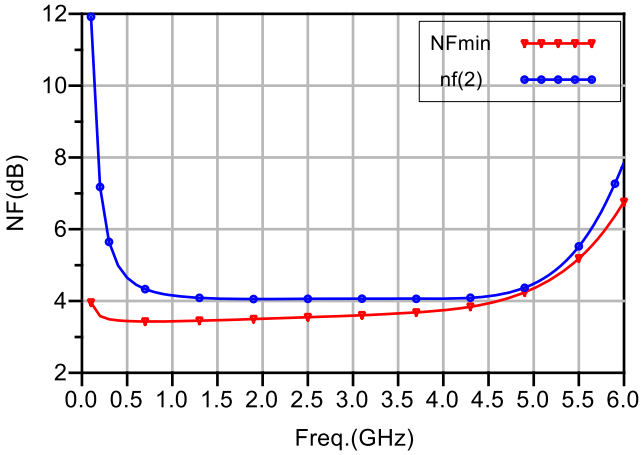

FIGURE 6.14: Noise Figure simulation result of resistive feedback inverter with Lg LNA.

6.4.3 Comparison of with and without Lg LNA Design

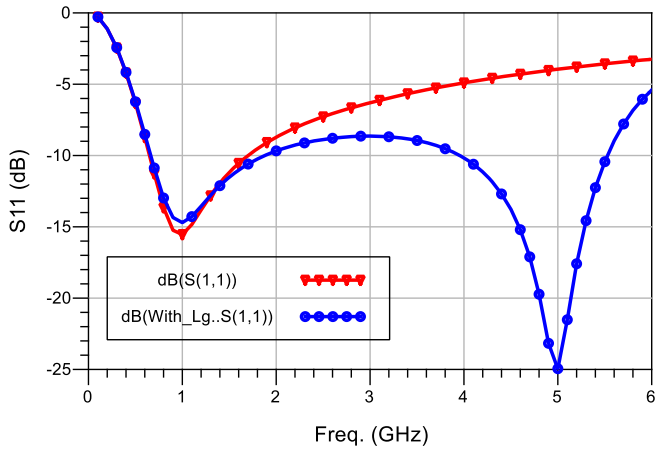

FIGURE 6.15: S_{11} simulation results of with and without Lg resistive feedback inverter LNA.

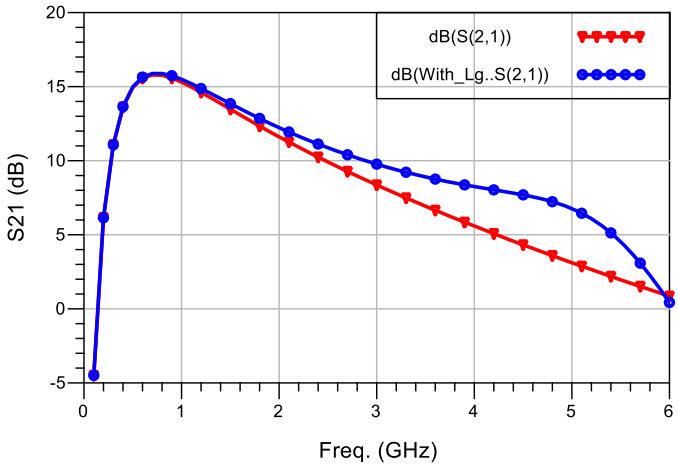

FIGURE 6.16: S_{21} simulation results of with and without Lg resistive feedback inverter LNA.

Simulation result of the matching (S_{11}) and power gain (S_{21}) are shown in Fig. 6.15 and Fig. 6.16 respectively. With gate inductor design improves input matching (S_{11}) and power gain (S_{21}) at higher frequency compare to without gate inductor resistive feedback inverter design. Gate inductor improves matching and gain at higher frequency by nullifying input capacitance effect.

6.5 Resistive and CD Feedback Inverter Wideband LNA

In [74] CMOS inverter feedback resistance adds thermal noise. Lower feedback resistance for wideband input matching is preferable but it increase noise figure of the design. There is tread off between low noise figure and wideband input matching: higher value of

feedback resistor decrease NF but it does not provide wider band input matching and vice versa [74]. Common drain (CD) active feedback in resistive feedback inverter is relax tradeoff between NF and matching by proving one more degree of freedom to set independently NF and input impedance. CD feedback also improve noise figure by cancelling out off phase noise signals. Adding CD feedback stage, consumes extra power. Schematic of resistive and CD feedback inverter LNA is shown in Fig. 6.18.

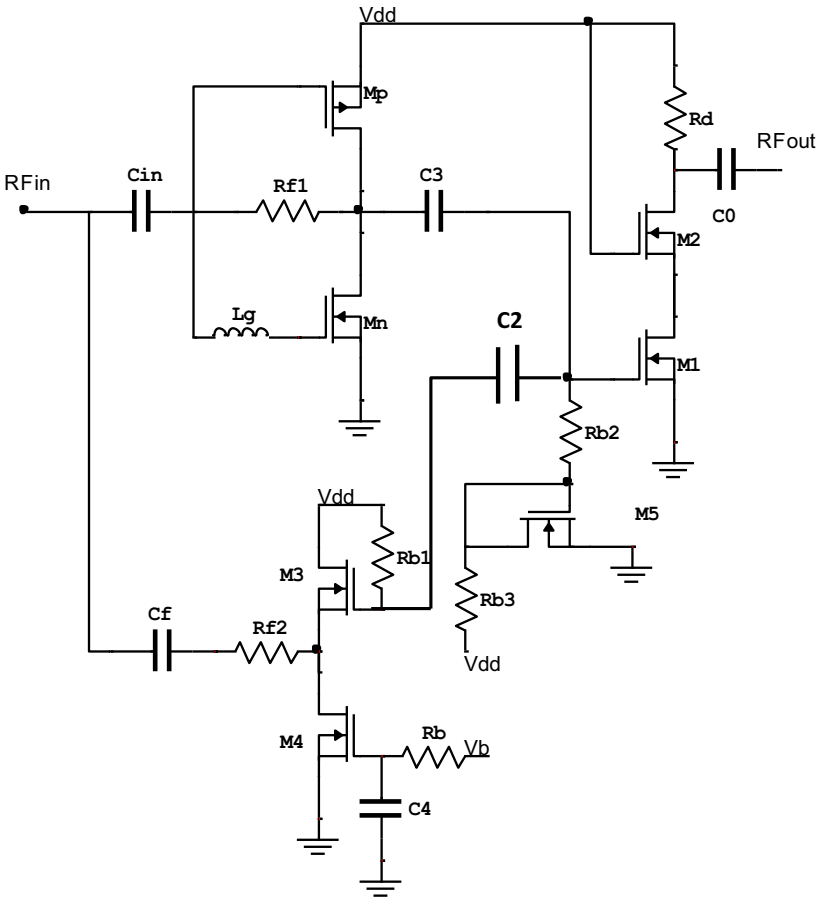

FIGURE 6.17: Resistive and CD feedback inverter wideband LNA schematic.

6.5.1 Common Drain (CD) Feedback Analysis

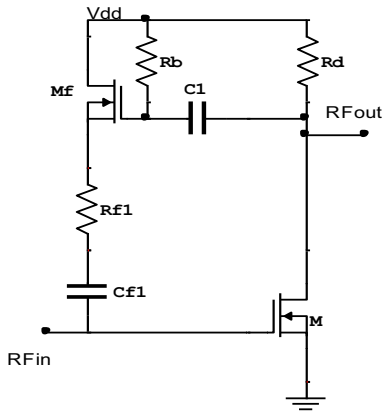

FIGURE 6.18: CS with common drain active feedback schematic.

By applying KCL at Vout and Vin node the expression for the voltage gain is obtained as

$$V_{out} = I_{d,in}R_L = -g_{m,in}R_L V_{in} \tag{6.25}$$

$$A_v = \frac{V_{out}}{V_{in}} = -g_{m,in}R_L \tag{6.26}$$

Feedback current I_{df} can be found by applying KVL in feedback loop

$$I_{d,f} = g_{m,f}(V_{out} - (V_{in} + I_{d,f}R_f)) \tag{6.27}$$

$$= -g_{m,f}((1 + g_{m,in}R_L)V_{in} + I_{d,f}R_f$$

$$I_{d,f}(1 + g_{m,f}R_f) = -g_{m,f}(1 - A_v)V_{in} \quad \therefore A_v = -g_{m,in}R_L \tag{6.28}$$

$$I_{d,f} = \frac{-g_{m,f}(1-A_v)V_{in}}{(1+g_{m,f}R_f)} \tag{6.29}$$

$$I_{in} = -I_{d,f} = \frac{g_{m,f}(1-A_v)V_{in}}{(1+g_{m,f}R_f)} \tag{6.30}$$

Using (6.25), (6.26) and (6.30) input impedance simplify as

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1+g_{m,f}R_f}{g_{m,f}(1-A_v)} \cong \frac{R_f}{-A_v} \tag{6.31}$$

As with a purely resistive feedback gm of the input device sets the input impedance but now the impedance is scaled by R_F and R_L. The system is of course even more complex, transistors add capacitances in the signal path and the cancellations stage add capacitance to the load of the input stage and to the input of the LNA.

TABLE 6.4: Components value of resistive and CD feedback inverter wideband LNA design.

Component	Value	Component	Value
W_n	6.4x30 µm	Rf1	50 KΩ
W_p	6.4x30 µm	Rf2	400 Ω
W_1	7x30 µm	Cin, C2,C3, Cout,C4	2.0 pF
W_2	7x30 µm	Vdd	1.2 V
W_3	3.6x30 µm	Rb, Rb1, Rb2,	2.0 KΩ
W_4	2.7x20 µm	Rb3	1.0 KΩ
W_5	1.5x15 µm	Rd	50 Ω
Cf	1.0 pF	Lg1	1.75 nH

6.5.2 Simulation Results and Discussion

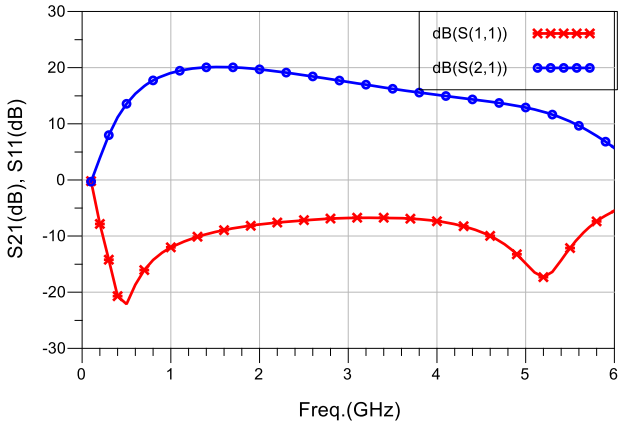

FIGURE 6.19: S_{21} and S_{11} simulation results of resistive and CD feedback inverter LNA.

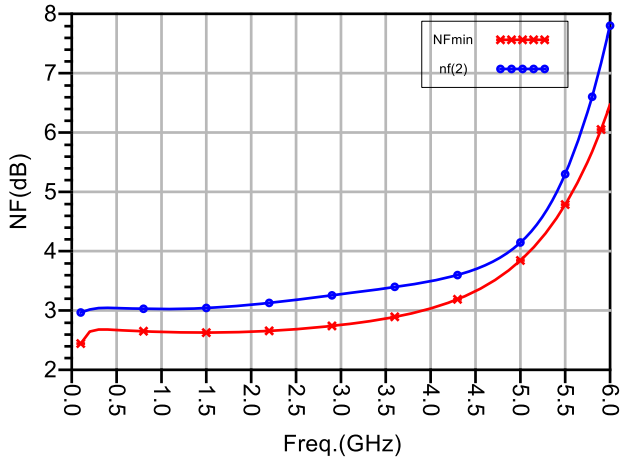

FIGURE 6.20: Noise Figure simulation result of resistive and CD feedback inverter LNA.

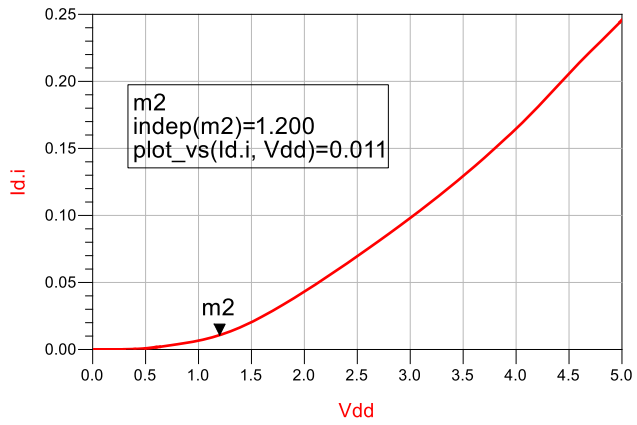

FIGURE 6.21: DC simulation result of resistive and CD feedback inverter LNA.

Simulation result of NF shows NF is decrease in resistive and CD feedback compared to single resistive feedback LNA in interested band. DC simulation result shows, introducing CD feedback consume 11 mA total current which is only 4 mA extra compare to resistive feedback inverter wideband LNA.

Series and shunt inductive peaking cascode CS next stage with resistive and CD feedback inverter structure will improve performance of LNA. The proposed highly linear multi standard wideband LNA design is based on resistive and CD feedback inverter with series and shunt peaking next stage.

6.6 Proposed Highly Linear Multi Standard Wideband LNA

Schematic of the proposed highly linear wideband based on dual negative feedback inverter structure with next stage series and shunt inductive peaking CS is shown in Fig. 6.23.

6.6.1 Design Analysis

The first stage of proposed highly linear wideband LNA is consisting resistive and common drain feedback to provide wideband input matching and low noise figure. Second stage is CS with series and shunt peaking inductors to improve overall gain and bandwidth of LNA. Value of coupling capacitor C3 and inductor Lg2 is to be selected such that it resonance at middle of interested band. Drain inductor Ld extend the bandwidth and improve the gain at high frequency [92].

TABLE 6.5: Components value of proposed highly linear multi standard wideband LNA design.

Components	Value	Components	Value
W_n	7.4x30 µm	Rf1	50 KΩ
W_p	8x30 µm	Rf2	220 Ω
W_1	6.8x64 µm	Cin, C2, C3, Cout,C4	2.0 pF
W_2	6.8x64 µm	Vdd	1.2 V
W_3	3.6x30 µm	Rb, Rb1, Rb2,	2.0 KΩ
W_4	8x15 µm	Lg1	1.71 nH
W_5	1.5x30 µm	Lg2	0.62 nH
Cf	1.0 pF	Ld	1.95 nH
Rb3	1.0 KΩ		

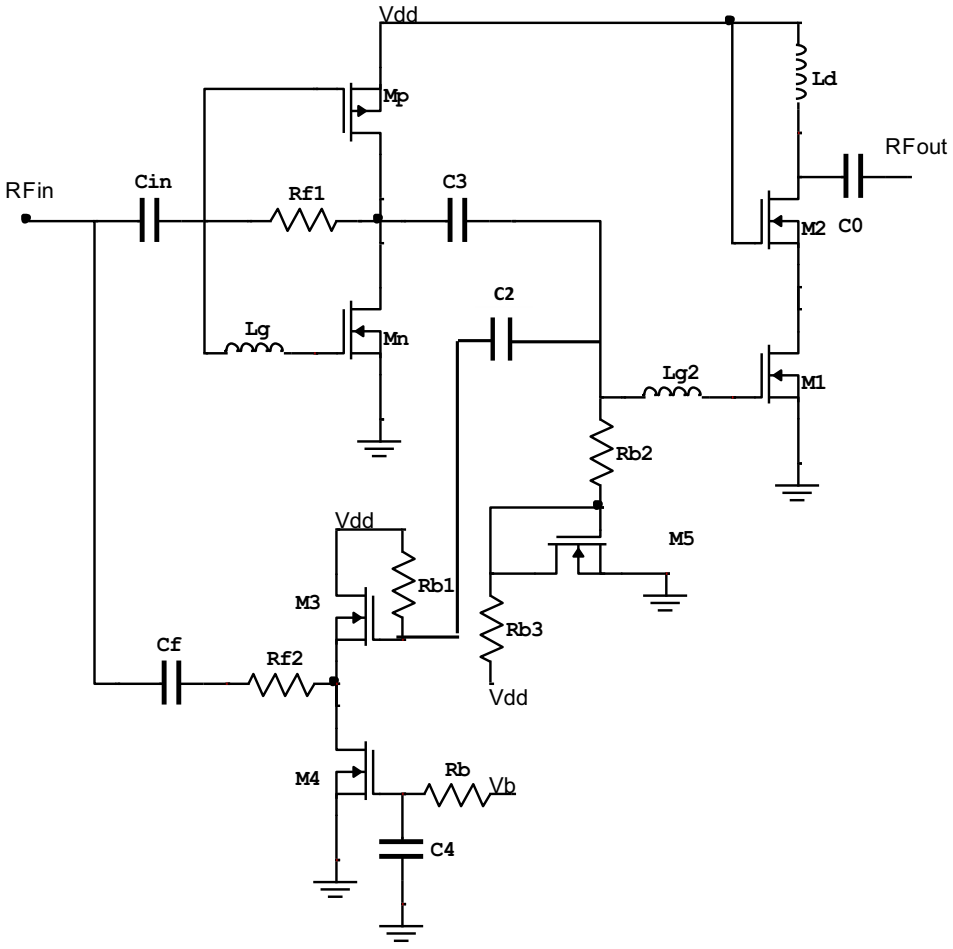

FIGURE 6.22: Proposed highly linear multi standard wideband LNA circuit.

6.6.2 Layout of Design

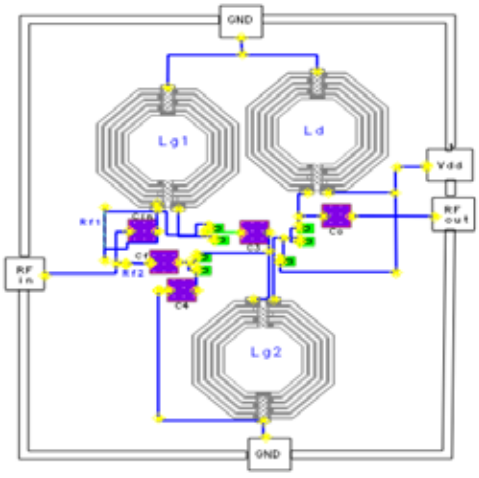

FIGURE 6.23: Layout of proposed highly linear multi standard wideband LNA.

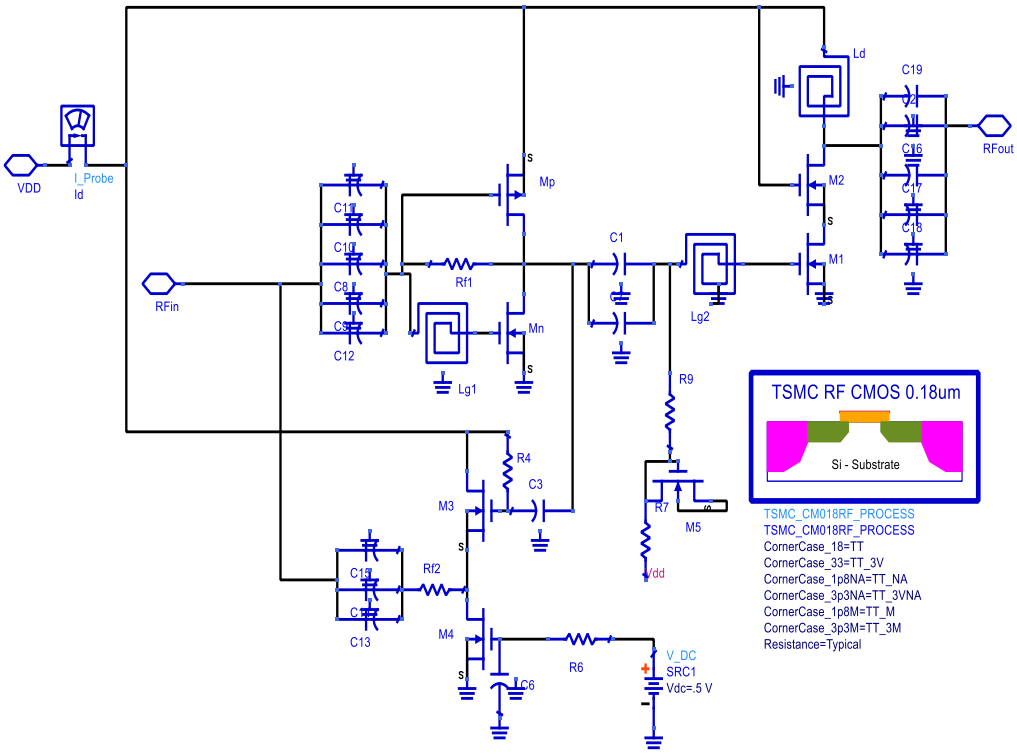

FIGURE 6.24: Highly linear wideband LNA schematic

6.6.3 Simulation Results and Discussion

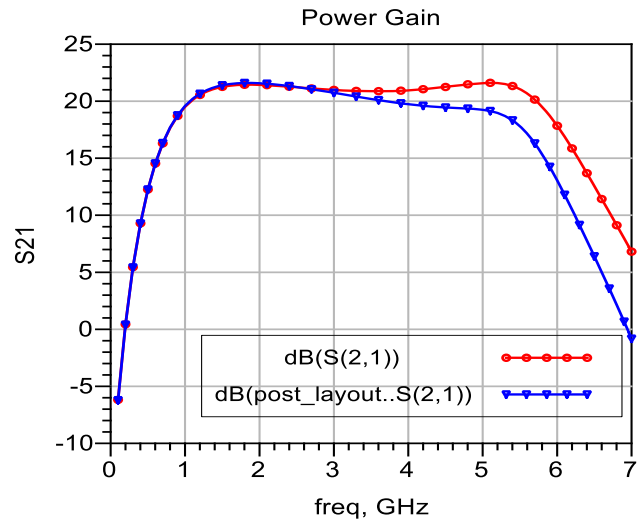

FIGURE 6.25: S_{21} simulation result of highly linear wideband LNA.

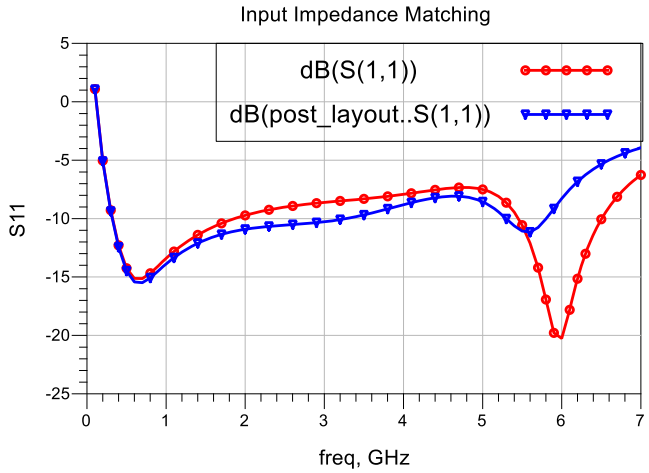

FIGURE 6.26: S_{11} simulation result of highly linear wideband LNA.

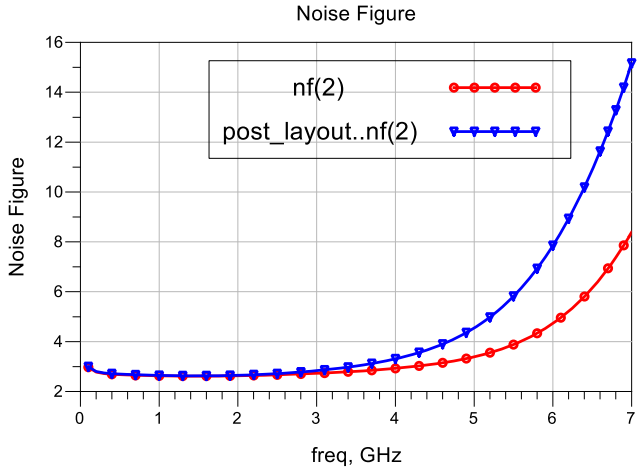

FIGURE 6.27: Noise figure simulation result of highly linear wideband LNA.

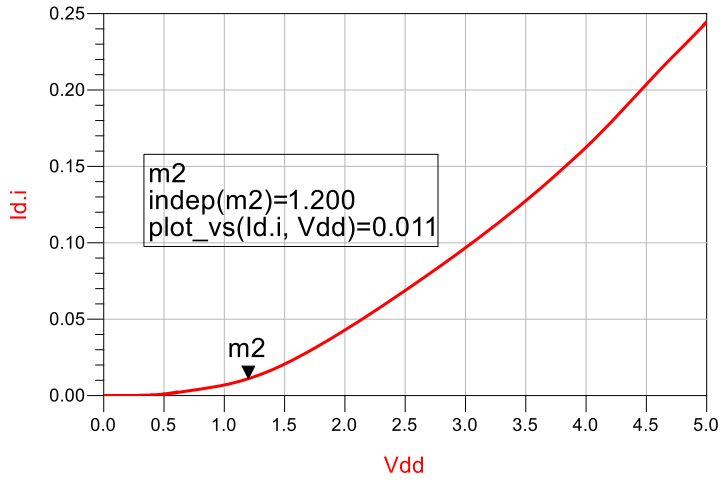

FIGURE 6.28: DC simulation result of highly linear wideband LNA.

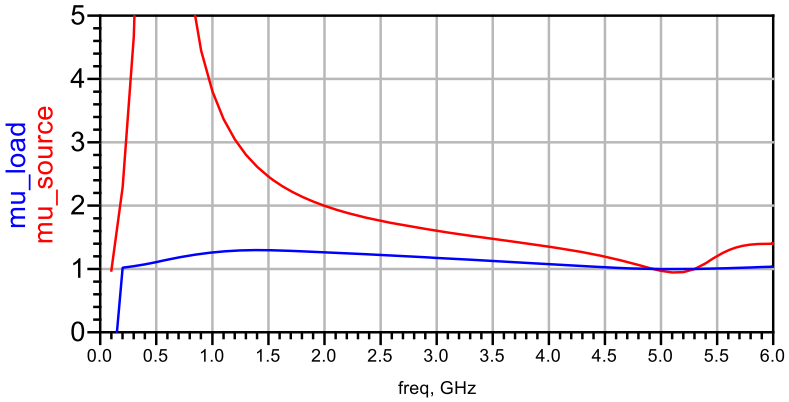

FIGURE 6.29: Stability factor simulation result of highly linear wideband LNA.

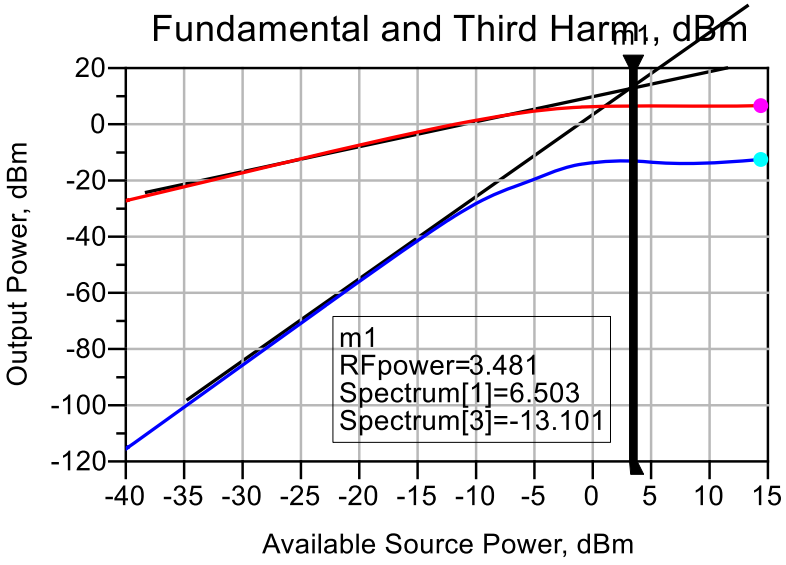

FIGURE 6.30: Harmonic simulation @3GHz result of highly linear wideband LNA

TABLE 6.6: IIP3 value of highly linear multi standard wideband LNA design at different frequencies.

Freq. (GHz)	IIP3 (dBm)
1	0.5
2	1
3	3.4
4	4.8
5	4.4
5.5	4.2

Simulation results of S_{21}, S_{11} and NF show the design has flat more than 20 dB power gain, less than -9 dB input reflection coefficient and less than 4 dB noise figure in 0.6-5.6 GHz interested band. Harmonic simulation result shows this design achieve very good linearity. Fig. 6.30 shows harmonic simulation result at 3 GHz, achieved IIP3 3.4 dBm @3GHz. Table 6.6 shows IIP3 value at different frequencies. The design achieved excellent average IIP3 is +4 dBm in interested band. DC simulation result shows the design consume only 13 mW power from 1.2 V supply. Due to low power consumption and good performance of the design make its highly suitable for next generation mobile terminal universal receiver.

6.7 High Power Gain Multi Standard Wideband LNA

Topology used to design high power gain wideband LNA is same as proposed for high power gain UWB LNA in chapter 5. Input and output matching for interested band is set by tuning inductors value.

6.7.1 Proposed LNA Schematic

TABLE 6.7: Components value of high power gain wideband LNA.

Components	Value	Components	Value
W_1	6x64 µm	Ls	5.9 nH
W_2	5x64 µm	Ld1	2.7 nH
W_3	5x64 µm	Ld2	5.6 nH
W_4	5x64 µm	Ld3	1.8 nH
W_5	5x64 µm	Vb1	0.53 V
W_6	2x20 µm	Vb2	0.61 V
W_7	1.5x40 µm	Vdd	1.2 V
Rf	6.0 kΩ	C1,C2,C3	1.0 pF

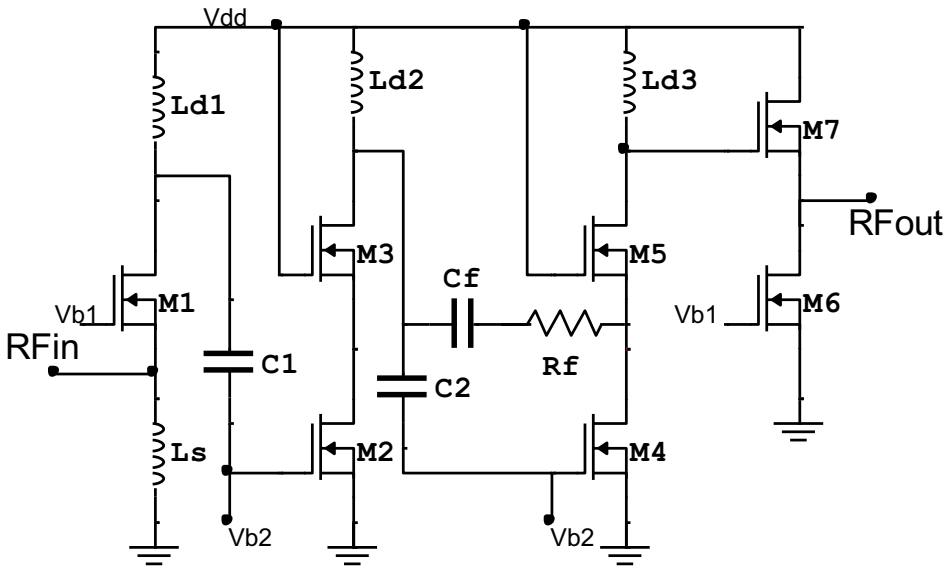

FIGURE 6.31: High power gain wideband LNA schematic.

6.7.2 Layout of the Design

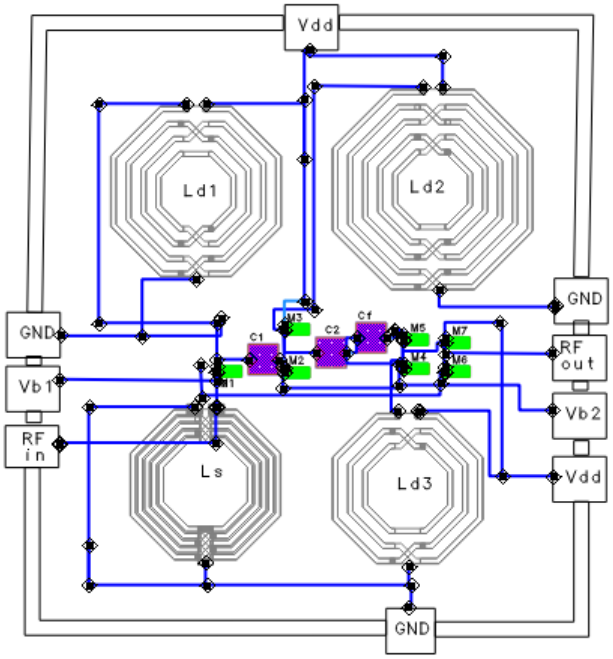

FIGURE 6.32: Layout of high power gain wideband LNA.

6.7.3 Simulation Results

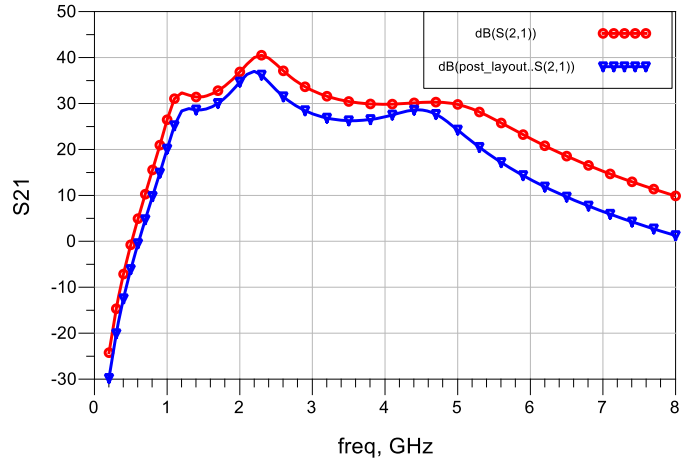

FIGURE 6.33: S_{21} simulation result of high power gain wideband LNA.

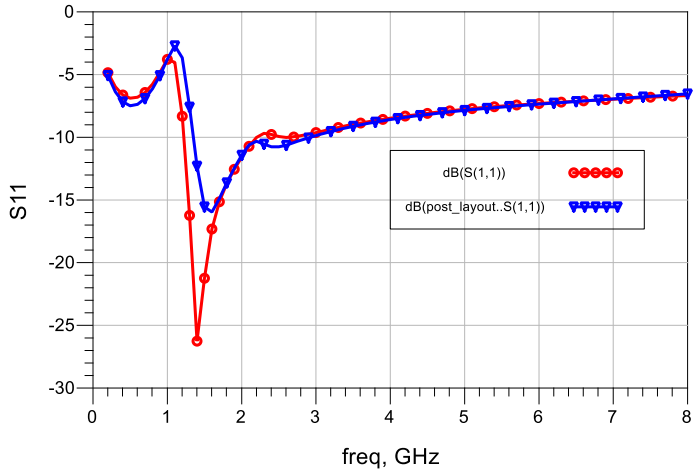

FIGURE 6.34: S_{11} simulation results of high power gain wideband LNA.

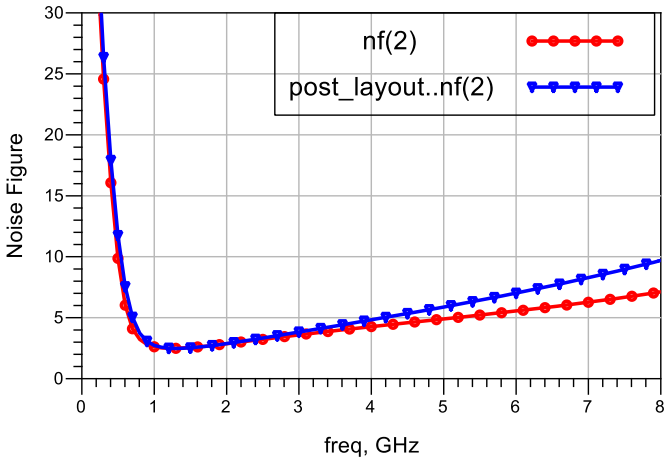

FIGURE 6.35: Noise Figure Simulation result of high power gain wideband LNA.

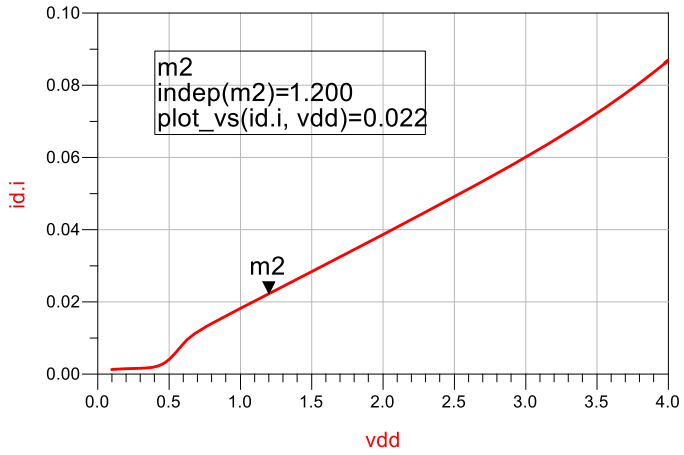

FIGURE 6.36: DC Simulation result of high power gain wideband LNA.

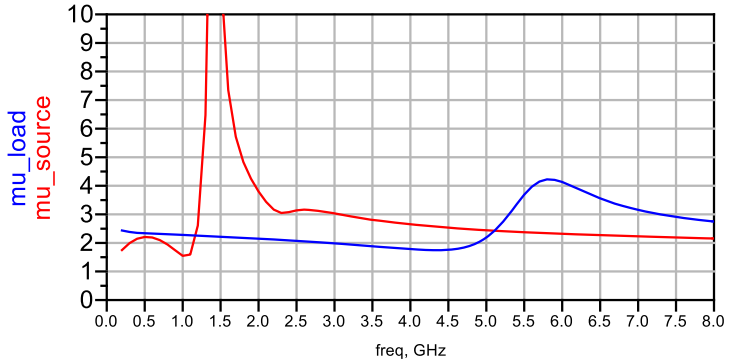

FIGURE 6.37: Stability simulation of high power gain wideband LNA.

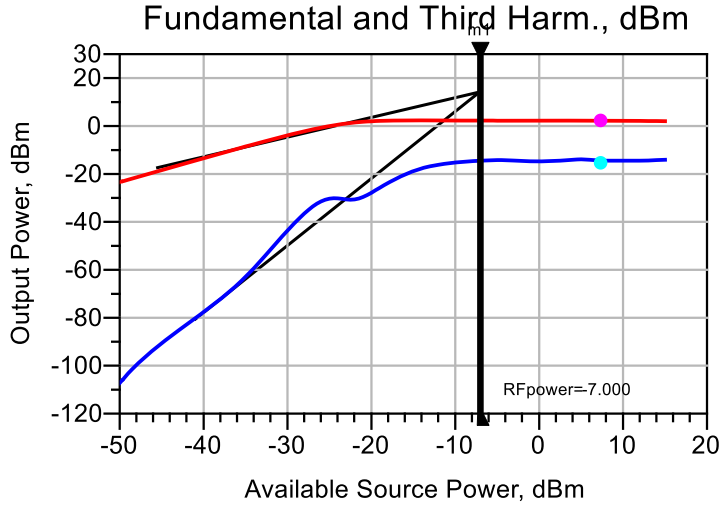

FIGURE 6.38: Harmonic simulation @3 GHz of high power gain wideband LNA.

Simulation results shows the high power gain wideband LNA design achieved average 30 dB power gain, less -8 dB input reflection coefficient and less 5 dB noise figure in interested 0.6-5.6 GHz band. DC simulation shows the design is consuming 26 mW power

including bias circuit from 1.2 V supply. Harmonic simulation result shows the design having -7 dBm IIP3 at 3 GHz. The stability simulation show the design is unconditionally stable even having very high gain.

The proposed high power gain multi standard wideband LNA design have very high power gain with good matching and noise figure in interested band. This design is consuming slightly higher power due to multistage. Table 6.8 shows the comparison of proposed design results with recently published work. The high power gain wideband LNA design is highly suitable for base station RF universal receiver.

FOM of the different designs has been calculated as per 3.34. Figure 4.39 shows proposed highly linear wideband LNA achieved 50.75. FOM of the design specified in paper [71] is highest 66.72 but its 3 dB higher cutoff frequency is 1.77 GHz which not supports 1.77-5.6 GHz band wireless standards. Another high power gain proposed LNA design achieved 30.5 FOM.

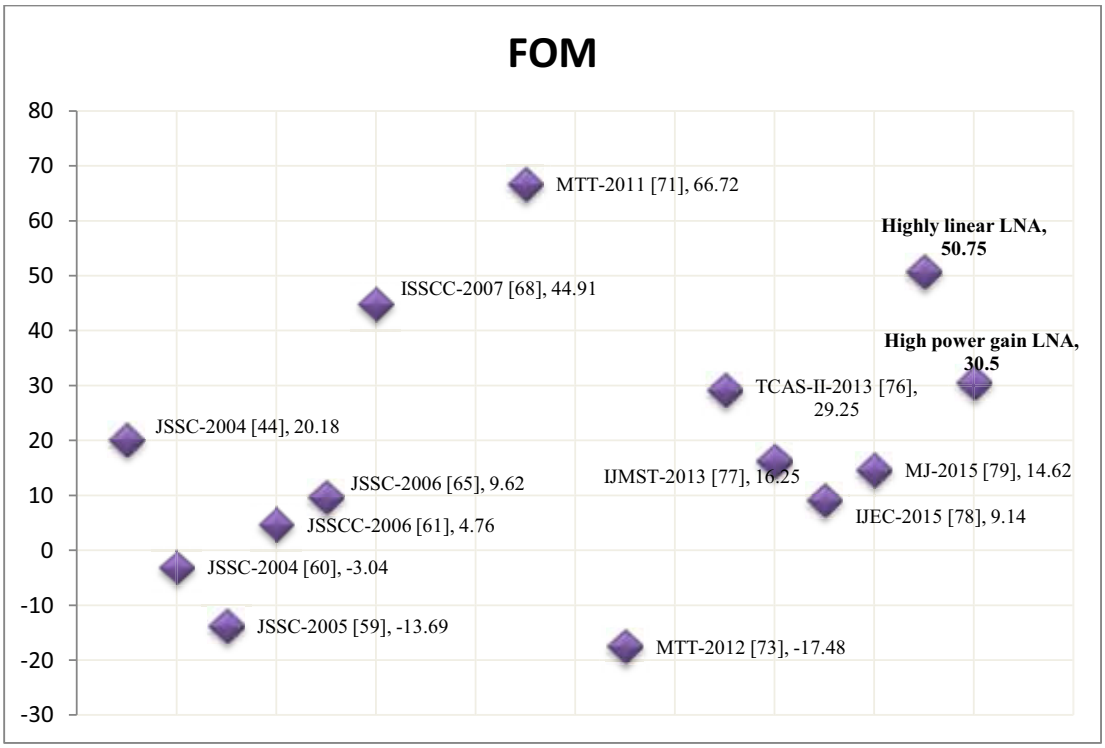

FIGURE 6.39: FOM comparison of proposed work with published wideband LNAs.

TABLE 6.8: Comparison of proposed wideband LNAs results with published work.

Source	CMOS Technology (um)	BW (GHz)	S_{21} (dB)	S_{11} (dB)	NF (dB)	IIP3 (dBm)	Power Consumption (mW)	Area (mm^2)	Topology	FOM
JSSC-2004 [44]	0.25	0.002-1.6	13.7	<-8	2.4	0	35	0.075	R FB +NMOS/PMOS	20.18
JSSC-2004 [60]	0.18	2.3-9.2	9.3	<-10	4	-6.7	9	0.66	CS + degeneration and input BPF	-3.04
JSSC-2005 [59]	0.18	2-4.6	9.8	<-9	2.3	-7	12.6	0.9	CS + series RC FB	-13.69
JSSCC-2006 [61]	0.18	3-5	<16	-10.5	2.2	-9	7.68	0.63	CS with Input matching filter	4.76
JSSC-2006 [65]	0.18	0.04-7	8.6	<-16	4.2	+3	9	1.16	Distributed cascode	9.62
ISSCC-2007 [68]	0.13	1-7	17	<-10	2.4	-4.1	25	0.019	Cascode + CD FB	44.91
MJ-2008 [69]	0.18	5-6	20.5	-21.3	1.8-2.6	-6.2	2	-	Cascode + inter stage LC network	-
ISSCC-2009 [37]	0.18	0.3-0.92	21		2	-3.2	3.6	-	Differential CG + C Cross coupling	-
MTT-2011 [71]	0.09	0.01-1.77	23	<-10	2	-2.85	2.8	0.03	Differential CG + multiple f/b	66.72
IET MAP 2012 [72]	0.18	2.4-11.2	14.8	-	3.9	-11.5	3.4	-	CG + current reuse	-
MTT-2012 [73]	0.13	0.6-3	42v	<-8	3	-14	30	1.5	Pseudo differential + resistive FB	-17.48
MWCL-2012 [75]	0.065	0.01-2.8	32v	-	1	-13.6	40	-	Cascode + active –C element	-
TCAS-II-2013 [76]	0.18	0-1.3	10	<-10	3	+7.5	18	0.07	Cascode + active feedback	29.25
IJMST-2013 [77]	0.18	2.5-16	11	<-7	3.3	-5	20	0.18	RC FB CS + current reuse	16.25
IJEC-2015 [78]	0.13	2.35-9.37	10.3	<-8	3.68	-4	9.97	0.39	CG current resue + noise cancelling	9.14
MJ-2015[79]	0.13	3.5-5	14	<-15	3.5-3.9	4	21	0.31	Fully differential + active FB + Noise cancelling	14.62
Hihgly linear wideband LNA	**0.18**	**0.6 – 5.6**	**16-21**	**<-10**	**<3.2**	**+ 4 average**	**13.2**	**0.09**	**Resistive + CD feedback Inverter**	**50.75**
High Power gain wideband LNA	**0.18**	**0.6 - 5.6**	**20-34**	**<-8**	**4-6**	**-7 @3 GHz**	**26**	**0.18**	**CG + Cascaded CS**	**30.5**

TABLE 6.9: Wireless Standards.

Standard	Description	Access techniques	Modulation types	Frequency Band Tx/Rx(MHz)	Channel Spacing (MHz)	Data Rate (Mb/s)
GSM	Cellular 2G (digital voice, SMS)	TDMA/ FDMA/ FDD	GMSK	890-915/935-960	0.2	0.27
DCS-1800	Cellular 2G (digital voice, SMS)	TDMA	GMSK	1710-1785/1805-1850	0.2	0.27
PCS-1900	Cellular 2G (digital voice, SMS)	TDMA	GMSK	1880-1910/1930-1955	0.2	0.27
IS-95	Cellular 2G (digital voice, SMS)	CDMA	OQPSK	824-849/869-894	1250	1.228
EDGE	Cellular 2.5 G (higher capacity package data)	TDMA	GMSK/98-PSK	1850-1910/1930-1990	0.2	0.27
GPRS	Cellular 2.5 G (higher capacity package data)	TDMA	GMSK	880-915/925-960	0.2	0.27
WCDMA (UMTS)	Cellular 3G (Voice Multimedia, broadband internet access)	CDMA	QPSK	1920-1980/2110-2170	5	3.84
HSDPA	Cellular 3.5G (High speed downlink uplink packet access)	OFDM/ MIMO	QAM	1920-1980/2110-2170	5	14.4
HSUPA	Cellular 3.5G (High speed downlink uplink packet access)	OFDM/ MIMO	QAM	1920-1980/2110-2170	5	5.76
Bluetooth (IEEE 802.11 FH)	Personal area network	CDMA/FH	GFSK	2400-2482	1	1
ZigBee	Personal area network	CDMA/FH	GFSK	2402-2482	5	0.02,0.04 ,0.25
UWB	Personal area network		SP/FS	3100-10600	500	110-480
IEEE 802.11a	Wireless local area network (WLAN)	OFDM	BPSK	5000	16.26	6-54
IEEE 802.11b	WLAN	DSSS	D-BPSK/ D-QPSK	2400	22	1-11
IEEE 802.11g	WLAN	DSSS	D-BPSK /D-QPSK	2400	16.25-22	1-54
IEEE 802.11n	WLAN	OFDM/ MIMO	QAM	2400-5000	22	>100
IEEE 802.16d/e	Metropolitan area network (WiMAX)	OFDM/ MIMO	BPSK/ QPSK/ QAM	2400-11000	28	>1000 (Stationary), >100 (mobile)
LTE	4G, GPP	OFDMA/ MIMO/ SC-FDMA	QPSK/ 16QAM/ 64QAM	1850 – 1910 /1930 – 1990, 1710 – 1785 /1805 -1880, 1710 – 1755/ 2110 - 2155	20	100,150, 300(downlink), 50,75(upl in)

CHAPTER 7

Conclusions, Major Contributions and Scope of Future Work

7.1 Conclusions and Major Contributions

In this thesis Proposed, Analyzed and Designed wideband and narrowband LNAs for improve performance of RF receiver for fulfill need of future wireless communication. The performance parameters of the LNA, Input/output impedance matching, noise figure, gain and linearity have tradeoff among them. The proposed designs aim to relax tradeoff among different performance parameters and improve performance of the LNA to make it suitable for future RF receiver.

Chapter 4 presented the detail design of the LNAs for Bluetooth and GPS applications. The first LNA was designed using inductive degenerate topology for Bluetooth receiver and it's achieved power gain (S_{21}), input reflection coefficient (S_{11}), NF and IIP3 is 22 dB, -21 dB, 3.6 dB and 1 dBm respectively. The LNA design consumed 10.8mW power from 1.8V supply. Bluetooth receiver LNA is also designed using current reuse LNA topology for portable low power devices. The proposed CRLNA design consuming only 5.4 mW power from 1.8V supply voltage which saved 50% power compare to simple inductive degenerate topology with the cost of larger silicon area. The 1.575 GHz narrowband LNA for GPS receiver is designed using inductive degenerate topology. The LNA for GPS receiver achieved Power gain, S_{11}, NF, IIP3 and power consumption are 20 dB, -20 dB, 3 dB, 1 dBm and 10.8 mW respectively. The proposed narrowband LNA designs will improve performance of future Bluetooth and GPS wireless communication.

Chapter 5 presented detailed design, analysis and simulation of high power gain 3.1- 10.6 GHz ultra wideband LNA for UWB system. The proposed UWB LNA design optimized for specifically high power gain for UWB RF frontend receiver. Due to FCC restriction, low power transmission for commercial UWB wireless applications require low noise high power gain receiver to amplify and process received weak signals. Common gate configuration of first stage of proposed design provided wideband input impedance matching in the multistage UWB LNA design. The CG has low power gain. The power gain has improved by using two cascade CS stages after CG in the proposed LNA design. NF and gain of the design have improved due to inductive load used instead of resistive in the design. Inductive load and next stage input capacitor are formed parallel tune circuit. Bandwidth of the design has improved by resonant each parallel tune circuit at different frequencies in interested band.

Simulated results of the UWB LNA design showed maximum power gain is 20-30 dB in interested band with low noise figure 2.8-6 dB. The achieved S_{11} and IIP3 of the UWB LNA have -9 dB and -5.5 dBm respectively in interested band. Due to multi stage the proposed UWB LNA design has consumed slightly more power, 34 mW from 1.5V supply. Results of the high power gain UWB LNA shows the design has improved performance and makes it suitable for future UWB system and will open new frontier for UWB wireless communication users. FOM of proposed design shows UWB LNA achieved worthy overall performance with higher power gain compare to literature works.

In the chapter 6 highly linear 0.6-5.6 GHz wideband LNA designs for multi standards universal receiver are discussed. The proposed 0.6-5.6 GHz wideband matching, high linearity, high gain and low noise figure LNA design will support LTE and WiMAX 4G standards with existing GSM, CDMA, UMTS, Bluetooth, ZigBee and WLAN wireless standards for future RF receiver.

The first multi standard highly linear wideband LNA design is based on NMOS/PMOS inverter structure. The complementary characteristic of NMOS and PMOS transistors have improved linearity of the design by cancelling distortion. Resistive feedback NMOS/PMOS inverter structure is widely used in literature for linear wideband LNA design. Inverter structure of amplifier increased gain and reduced power consumption by current reusing but due to its higher input capacitance it reduced gain at higher frequency. Gate inductor based design has improved input impedance matching and gain at higher

frequency by cancelling capacitive effect. CD active feedback with resistive in NMOS/PMOS inverter structure has relaxed tradeoff among noise figure and input matching by providing one more degree of freedom to set input impedance matching and noise figure independently. The proposed highly linear wideband LNA has shunt and series inductive peaking CS next stage with CD active and resistive feedback NMOS/PMOS inverter structure.

Highly linear wideband LNA design achieved S_{21}, S_{11}, NF and average IIP3 were 16-20 dB, -10 dB, 3.2 dB and +4 dBm respectively. The design consumes 13.2 mW power including bias circuit. Stability simulation result showed that the design is unconditionally stable in interested band. Performance of the proposed highly linear wideband LNA makes it highly suitable for next generation 4G multi standards mobile terminal.

The next 0.6 – 5.6 GHz wideband LNA is designed for high power gain multi standards universal receiver. The high power gain multi standard wideband LNA is designed using CG with multi stage CS topology. The high power gain wideband LNA design achieved S_{21}, S_{11}, NF, IIP3 were >20 dB, <-8 dB, 4-6 dB and >-7 dBm respectively in interested 0.6-5.6 GHz band. Due to multistage the design consumed slightly high power, 26 mW including bias circuits. FOM shows proposed multi standards LNAs design achieved good overall performance compare to published wideband LNA designs.

All the LNAs were designed using TSMC 0.18μm RFCMOS technology. The proposed three novel wideband LNA topologies are relaxed tradeoff and improved performance of LNA. The high power gain with wideband matching and low noise figure UWB LNA design will improve performance of the UWB receiver. The highly linear and high power gain multi standard wideband LNA design will improve performance of future wireless communication.

7.2 Scope of Future Work

Here the work performed pre and post layout simulation to validate proposed LNAs design. In future, design will fabricate and validate for suitability for future wireless receiver.

The fabrication of passive inductor requires larger silicon area and it is not scalable as technology scale. Various active inductor design techniques are specified in literature. Active inductor based LNA design requires less silicon area and design is scalable but it adds more noise and consumes more power compared to passive inductor design. The NF and power consumption of active inductor based LNA can be reduce by using noise cancelling and low power LNA design.

RF frontend have three main analog blocks LNA, Mixer and Local oscillator. The work is expand by the design of mixer and local oscillator for multi standard universal receiver and integrate proposed LNA design with mixer and local to make complete RF frontend.

List of References

[1] J. Mitiola (1995) "The software radio architecture", IEEE Communication Mag., vol. 33 (5) pp. 26-38.

[2] M. Brandolini, P. Rossi, D. Manstretta, and F. Svelto, (2005), "Toward multi-standard mobile terminals fully integrated receivers requirements and architectures", IEEE Tran. Microwave Theory and Tech., vol. 53 (3) pp. 1026–1038.

[3] T. H. Lee, (1998), *"The Design of CMOS Radio-Frequency Integrated Circuits"*, 2nd ed., Cambridge University Press, Cambridge, U. K.

[4] B. Razavi, (2000), *"Design of Analog CMOS Integrated Circuits"*, McGraw-Hill.

[5] A. Van Der Ziel, (1962), "Thermal noise in field-effect transistors", Proceeding of IRE, vol. 50 (8) pp. 1808–1812.

[6] Y. Tsividis, (2003), *"Operation and Modeling of the MOS Transistor"*, 2nd Edition. Oxford University Press.

[7] Y. J. Wangand and A. Hajimiri, (2009), "A compact low-noise weighted distributed amplifier in CMOS", *Proceedings of the IEEE International Solid State Circuits Conference*, pp.220–222.

[8] A. Antonopoulos, M. Bucher, K. Papathanasiou, N. Mavredakis, N. Makris, R. K. Sharma, P. Sakalas, and M. Schroter, (2013), "CMOS Small-Signal and Thermal Noise Modeling at High Frequencies", IEEE Trans. Electron Devices, vol. 60 (11) pp. 3726–3733.

[9] A. Scholten, L. Tiemeijer, R. van Langevelde, R. Havens, A. Zegers-van Duijnhoven, R. de Kort, and D. Klaassen, (2004), "Compact modelling of noise for RF CMOS circuit design", IEEE Proceeding Circuits, Devices System, vol. 151, no. 2 (4) pp. 167-174.

[10] B. Razavi and K. Lee, (1994), "Impact of distributed gate resistance on the performance of MOS devices", IEEE Trans. Circuits Syst. I, vol. 41 (11) pp. 750– 754.

[11] R. Jindal, (2006), "Compact Noise Models for MOSFETs", IEEE Trans. Electron Devices, vol. 53 (9) pp. 2051-2061.

[12] B. Razavi, (1998), "RF Microelectronics" Prentice Hall.

[13] Z. Ru, E. A. M. Klumperink, C. E. Saavedra, and Bram Nauta, (2010), "A 300-800 MHz tunable filter and linearized LNA applied in a low-noise harmonic rejection RF sampling receiver", IEEE J. Solid-State Circuits, vol. 45 (5) pp. 967–978.

[14] A. Kruth, M. Simon, K. Dufrene, R. Weigel, Z. Boos, and S. Heinen, (2006), "A multimode receiver front-end for software defined radio", *in: Proceedings of 9th European Conference on Wireless Technology* (9) pp. 19–22.

[15] B. G. Perumana, J. H. C. Zhan, S. S. Taylor, B. R. Carlton, and J. Laskar, (2008),"Resistive feedback CMOS low-noise amplifiers for multiband applications", IEEE Trans. Microwave Theory Tech. vol. 56 (5) pp. 1218–1224.

[16] C. P. Moreira, E. Kerheve, P. Jarry and D. Belot, (2006), "A concurrent fully-integrated LNA for WLAN IEEE 802.11b/g/a applications", *Proceedings of 36th European Microwave Conference*, (9) pp. 1552–1555.

[17] M. Zargari, (2004), "A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/gWLAN", IEEE J. Solid-State Circuits, vol. 39 (12) pp. 2239-2249.

[18] O. E. Erdoganetal, (2005), "A single-chip quad-band GSM/GPRS transceiver in 0.18 μm standard CMOS", *IEEE International Solid-State Circuits Conference Digest of Technical Papers*.

[19] P. Zang and B. Razavi, (2005), "A single-chip dual-band direct conversion IEEE 802.11a/b/g WLAN transceiver in 0.18 mm CMOS", IEEE J. Solid-State Circuits, vol. 40 (9) pp. 1932–1939.

[20] S. Wu and B. Razavi, (1998), "A 900MHz/1.8GHz CMOS receiver for dual-band applications", IEEE J. Solid-State Circuits, vol. 33 (12) pp. 2178–2185.

[21] A. Liscidini, M. Brandolini, D. Sanzogni, and R. Castello, (2006), "A 0.13 μm CMOS frontend for DCS1800/UMTS/802.11b-g with multi band positive feedback low noise amplifier", IEEE J. Solid-State Circuits, vol. 41 (4) pp. 981–989.

[22] H. Hashemi and A. Hajimiri, (2002), "Concurrent multiband low-noise amplifiers theory, design and applications", IEEE Trans. Microwave Theory Tech., vol. 50 (1) pp. 288–301.

[23] J. Ryynanen, K. Kivekas, and J. Jussila, (2001), "A dual band RF frontend for WCDMA and GSM applications", IEEE J. Solid-State Circuits, vol. 36 (8) pp. 175–178.

[24] K. L. Fong, (1999), "Dual-band high-linearity variable-gain low-noise amplifiers for wireless applications", *IEEE International Solid-State Circuits Conference Digest*, February pp. 224–225.

[25] L. H Lu, H. H. Hsieh, and Y. S. Wang, (2005), "A compact 2.4/5.2-GHz CMOS dual band low noise amplifier", IEEE Microwave Wireless Components Letters, vol. 15 (10) pp. 685-687.

[26] Z. Li, R. Quintal, and K. O. Kenneth, (2004), "A Dual-band CMOS frontend with two gain modes for wireless LAN applications", IEEE J. Solid State Circuits, vol. 39 (11) pp. 2069–2073.

[27] B. M. Ballweber, R. Gupta, and D. J. Allstot, (2000), "A Fully Integrated 0.5 – 5.5 GHz CMOS Distributed Amplifier", IEEE Journal of Solid-State, vol. 35 (2) pp. 231-239.

[28] D. Manstretta, (2008), "A broadband low noise single ended input differential output amplifier with IM2 canceling", *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 79–82.

[29] P. J. Sullivan, B. J. Xavier, and W. H. Ku, (1997), "An integrated CMOS distributed amplifier utilizing packaging inductance", IEEE Trans. Microwave Theory Tech., vol. 45 (10) pp. 1817 – 1818.

[30] R. C. Liu, C. S. Lin, K. L. Deng and H. Wang, (2003), "A 0.5–14GHz 10.6dB cascode distributed amplifier", *Symposium on VLSI Circuits*, Digest of Technical Papers, pp.139–140.

[31] R. C. Liu, K. L. Deng and H. Wang, (2003), "A 0.6-22 GHz Broadband CMOS Distributed Amplifier", Digest of Technical papers in RFIC Symposium, pp. 103-106.

[32] S. F. Wang, Y. S. Hwang, S. C. Yan and J. J. Chen, (2011), "A new CMOS wideband low noise amplifier with gain control", Integration VLSI J., vol. 44 pp. 136-143.

[33] W. Chen, G. Liu, B. Zdravko, and A. Niknejad, (2008), "A highly linear broadband CMOS LNA Employing Noise and Distortion Cancellation", IEEE J. Solid-State Circuits, vol. 43 (5) pp. 1164-1176.

[34] H. P. Koringa and Dr. V. A. Shah,(2016), "Wideband Low Noise Amplifier for Next Generation Wireless RF Frontend: A Review Paper" in IJAREST International journal vol. 3 (1) pp. 116-125.

[35] A. Nieuwoudt, T. Ragheb, H. Nejati, and Y. Massoud, (2009), "Numerical design optimization methodology for wideband and multi-band inductively degenerated cascode CMOS low noise amplifiers", IEEE Trans. Circuits Syst. I Regular Paper, vol. 56 (6) pp. 1088 – 1101.

[36] Y. Lu, K. S. Yeo, A. Cabuk, J. Ma, M. A. Do, and Z. Lu, (2006), "A novel CMOS low noise amplifier design for 3.1–10.6GHz ultra-wide-band wireless receivers", IEEE Trans. Circuits System I Regular Paper, vol. 53 (8) pp. 1683- 1692.

[37] S. Woo, W. Kim, C. Lee, K. Lim, and J. Laskar, (2009), "A 3.6 mW Differential common gate CMOS LNA with positive negative feedback", *IEEE International Solid-State Circuits Conference*, pp.218–220.

[38] J. Kim, S. Hoyos, and J. Martinez, (2010), "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization", IEEE Trans. Microwave Theory Tech., vol. 58 (9) pp. 2340-2351.

[39] C. Liao and S. Liu, (2007), "A broadband noise-canceling CMOS LNA for 3.1–10.6 GHz UWB receivers", IEEE J. Solid State Circuits, vol. 42 (2) pp. 329-339.

[40] G. H. Z. Fatin, Z. D. Koozehkanani and H. Sjoland, (2010), "A technique for improving gain and noise figure of common-gate wideband LNAs", Analog Integrated Circuits Signal Processing pp. 239–244.

[41] H. Zhang, X. Fan and E. S. Sinencio, (2009), "A low-power, linearized, ultra-wideband LNA design technique", IEEE J. Solid-State Circuits, vol. 44 (2) pp. 320–330.

[42] D. E. Norton, (1975), "High dynamic range feedback amplifiers using lossless feedback" *Proceedings of IEEE Symposium on Circuits and Systems*, pp. 438–440.

[43] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, (2002), "Noise cancelling in wideband CMOS LNAs", *Digest of Technical Papers. ISSCC. 2002 IEEE International Solid-State Circuits Conference*, vol. 1,pp. 406- 407.

[44] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, (2004), "Wide-band CMOS low-noise amplifier exploiting thermal noise cancelling", IEEE Journal of Solid-State Circuits, vol. 39, (2), pp. 275 - 282.

[45] Y. H. Yu, Y. S. Yang, and Y. J. E. Chen, (2010), "A compact wideband CMOS low noise amplifier with gain flatness enhancement", IEEE J. Solid-State Circuits, vol. 45 (3) pp. 502–509.

[46] M. E. Nozahi, A. A. Helmy, E. S. Sinencio, and K. Entesari, (2010), "A 2–1100 MHz wideband low noise amplifier with 1.43 dB minimum noise figure", IEEE Radio Frequency Integrated Circuits Symposium., pp. 119–122.

[47] M. E. Nozahi, A. A. Helmy, E. S. Sinencio, and K. Entesari, (2011), "An inductorless noise cancelling broadband low noise amplifier with composite transistor pair in 90 nm CMOS technology", IEEE J. Solid-State Circuits, vol. 46 (5) pp. 1111–1122.

[48] J. H. Lee, C. C. Chen, H. Y. Wang, and Y. S. Lin, (2008), "A 2.5 dB NF 3.1–10.6 GHz CMOS UWB LNA with small group-delay-variation" *Proceedings of IEEE Radio Frequency Integrated Circuits Symposium*, pp.501–504.

[49] J. Jung, T. Yun and J. Choi, (2006), "Ultra-wideband low noise amplifier using a cascode feedback topology", Microwave Optical Technology Letter, vol. 48 (6) pp. 1102–1104.

[50] R. Gharpurey, (2005), "A broad band low noise front-end amplifier for ultra wideband in 0.13 μm CMOS", IEEE J. Solid State Circuits, vol. 40 (9) pp. 1983-1986.

[51] K. C. He, M. T. Li, C. M Lia, and J. H. Tarng, (2010), "Parallel RC feedback low noise amplifier for UWB applications", IEEE Trans. Circuits and System II Express Briefs, vol. 57 (8) pp.582-586.

[52] M. Vidojkovic, J. V. Tang, M. Sanduleanu, P. Baltus, and A. V. Roermund, (2007), "A broadband, inductorless LNA for multi-standard applications", *Proceedings of IEEE European Conference on Circuit Theory and Design*, pp. 260-263.

[53] M. Vidojkovic, M. Sanduleanu, J. V. Tang, P. Baltus, and A. V. Roermund, (2007), "A 1.2V, inductorless, broadband LNA in 90 nm CMOS" *LPIEEE Radio Frequency Integrated Circuits Symposium.*, pp. 53–56.

[54] Y. Soliman, L. MacEachern and L. Roy, (2005), "A CMOS ultra-wideband LNA utilizing a frequency-controlled feedback technique", *Proceedings of IEEE International Conference on Ultra-Wideband (ICU)*, pp.530–535.

[55] A. C. Heiberg, T. W. Brown, T. S. Fiez, K. Mayaram, (2011), "A 250mV, 352mW GPS receiver RF front-end in 130nm CMOS", IEEE J. Solid-State Circuits, vol. 46 (4) pp. 938–949.

[56] K. W. Tang, M. Khanpour, P. Garcia, C. Garnier, and S. P. Voinigescu, (2007), "65 nm CMOS, W-band receivers for imaging applications", *Proceedings of IEEE Custom Integrated Circuits Conference (CICC)*, pp.749–752.

[57] M. T. Reiha and J. R. Long, (2007), "A 1.2 V reactive feedback 3.1-10.6 GHz low-noise amplifier in 0.13 μm CMOS", IEEE J. Solid State Circuits, vol. 42 (5) pp. 1023–1033.

[58] S. Andersson, C. Svenson, and O. Drugge, (2003), "Wideband LNA for a Multistandard Wireless Receiver in 0.18μm CMOS," *Proceedings of the European Solid-State Circuits*, September, pp. 655–658.

[59] C. W. Kim, M. S. Kang, P. T. Anh, H. T. Kim, and S. G. Lee, (2005), "An ultra wideband CMOS low noise amplifier for 3–5 GHz UWB system", IEEE J. Solid-State Circuits, vol. 40 (2) pp. 544–547.

[60] A. Bevilacqua, A. Niknejad, (2004), "An ultra-wideband CMOS LNA for 3.1 to 10.6GHz wireless receivers", IEEE J. Solid-State Circuits, vol. 39 (12) pp. 2259–2268.

[61] H. Jin Lee, D. S. Ha, and Sang S. Choi, (2006), "A 3–5 GHz CMOS UWB LNA with input matching using miller effect", *IEEE International Solid-State Circuits Conference*, pp. 646-648.

[62] M. S. Jung, C. W. Kim, P. T. Anh, H. T. Kim, and S. G. Lee, (2005), "A 2.7–9.3 GHz CMOS wideband amplifier combined with high pass filter for UWB system", *in Proceedings of 7th International Conference on Advanced Communication Technology (ICACT2005)*, February pp.

[63] H. K. Chen, Y. S. Lin, and S. S. Lu, (2010), "Analysis and design of a 1.6-28 GHz compact wideband LNA in 90 nm CMOS using a π-match input network", IEEE Trans. Microwave Theory Tech., vol. 58 (8).

[64] H. L. Kao and K. C. Chang, (2008), "Very low power CMOS LNA for UWB wireless receivers using current reused topology", J. Solid State Electron, vol. 52 pp. 86–90.

[65] F. Zhang and P. R. Kinget, (2006), "Low-Power Programmable Gain CMOS Distributed LNA", IEEE J. of Solid State Circuits, vol. 41 (6) pp. 1333–1343.

[66] B. Machiels, P. Reynaert, and M. Steyaert, (2010), "Power efficient distributed low noise amplifier in 90 nm CMOS", *in Proceedings of the IEEE Proceedings of Radio Frequency Integrated Circuits Symposium*, pp. 131–134.

[67] P. Heydari, (2007), "Design and analysis of a performance optimized CMOS UWB distributed LNA", IEEE J. Solid State Circuits, vol. 42 (9).

[68] R. Ramzan, S. Andersson, J. Dabrowskiand and C. Svensson, (2007), "A 1.4 V 25 mWinductorless wideband LNA in 0.13 μm CMOS", *IEEE international Solid-State Circuits Conference*, pp. 424–425.

[69] S. Toofan, A. R. Rahmati, A. Abrishamifar, and G. RoientanLahiji, (2008), "Low power and high gain current reuse LNA with modified input matching and inter-stage inductors", Microelectronics J., vol. 39 (12) pp. 1534–1537.

[70] Y. Sheng Lin, C. Zhi Chen, H. Yu Yang, C. Chen, J. H. Lee, G. W. Huang, and S. S. Lu, (2010), "Analysis and design of a CMOS UWB LNA with dual RLC branch wideband input matching network", IEEE Trans. Microwave Theory Tech., vol. 58 (2).

[71] E Ahmed Sobhy, Ahmed A Helmy, S Hoyos, K Entesari, and E Sanchez Sinencio, (2011), "A 2.8 mW Sub 2 dB Noise Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback", in IEEE Trans. Of Microwave Theory and Techniques, Vol. 59 (12) pp. 3154-3161.

[72] J. Y. lee, H. K. Park, H. J. Chang, and T. Y. Yun, (2012), "Low Power UWB LNA with common gate and current reuse techniques", IET Microwave, Antennas Propagation., vol. 6 (7) pp. 793-799.

[73] X. Wang, J. Sturm, N. yan, X. Tan, and H. Min, (2012), "0.6-3 GHz Wideband Receiver RF Front-End With a Feed forward Noise and Distortion Cancellation Resistive Feedback LNA", IEEE Trans. On Microwave Theory and Techniques, vol. 60 (2) pp. 387-392.

[74] A. I. A. Galal, R. Pokharel, H. Kanaya, and K. Yoshida, (2012), "High Linearity technique for ultra wideband low noise amplifier in 0.18um CMOS technology", International Journal of Electronics and Communication (AEU), Elsevier, vol. 66, pp. 12-17.

[75] L. Belostotski, A. Madanayake, and L. T. Bruton, (2012), "Wideband LNA with an Active –C Element", IEEE Microwave and Wireless Components Letters, vol. 22 (10) pp. 524-526.

[76] DongguIm, (2013), "A +9 dBm output P1 dB Active Feedback CMOS Wideband LNA for SAW Less Receivers", IEEE Transaction on Circuits and Systems-II Express briefs, vol. 60 (7) pp. 377-381.

[77] K. Yousef, H. Jia, R. Pokharel, A. Allam, M. Ragab, H. Kanaya, and k. Yoshida, (2013), "CMOS Ultra-Wideband Low Noise Amplifier Design", International Journal of Microwave Science and Technology.

[78] S. Arshad, R. Ramzan, K. Khurram Muhammad, and Q. ulWahab, (2015), "A sub-10mW, noise cancelling, wideband LNA for UWB applications", International Journal of Electronics and Communications (AEU) Elsevier, vol. 69 pp. 109-118.

[79] A. Zoaei, and A. amirabadi, (2015), "A 130nm wideband fully differential linear low noise amplifier", Elsevier Microelectronics Journal, vol. 46 pp. 825-833.

[80] H. P. Koringa and Dr. V. A. Shah, (2015),"Design and Optimization of Narrow Band Low Noise Amplifier using 0.18µm CMOS"*in IEEE international conference of communication and networking,* pp. 100-106.

[81] Fernando Azevedo, Fernando Fortes and M. Joao Rosario, (2006) "A 2.4 GHz Monolithic Single-ended-Input/Differential-Output Low-Noise Amplifier," *SiRF 2006*, Jan. pp.

[82] B. liu, C. Wang, M. Ma, S. Guo, (2009) "An ultra-low-voltage and ultra-low-power 2.4 Ghz LNA design" radio engineering, vol. 18, no. 4, december 2009 pp. 527-531.

[83] A. V. Do, C. C. Boon, M. A Do, K. S Yeo and A. Cabuk. (2008) "A sub threshold LNA optimized for Ultra low power applications in ISM band," *IEEE trans. Microwave Theory Tech*., vol.56, pp. 286-292, Feb. 2008.

[84] Raghavendra Bhat and Dr. K C Narasimhamurthy (2014) "Low Noise Amplifier at 2.4 GHz for Zigbee in MOS 180nm Technology" International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering ISSN (Print) : 2320 – 3765 ISSN (Online): 2278 – 8875) Vol. 3, Issue 6, June 2014 Copyright to IJAREEIE www.ijareeie.com 9934

[85] M. Isikhan and A. Richter (2009) "CMOS low noise amplifiers for 1.575 GHz GPS applications" Adv. Radio Sci., 7, pp. 145–150.

[86] Low Li Lian , Norlaili Mohd Noh and Mohd Tafir Mustaffa (2011) "A dual-band LNA with 0.18-µm CMOS switches" 2011 IEEE Regional Symposium on Micro and Nano Electronics, pp. 172-176.

[87] Tan Thiam Loong, Awatif Hashim and Mohd Tafir Mustaffa (2011) "1.575 GHz to 2.48 GHz multi-standard low noise amplifier using 0.18-µm CMOS with on-chip matching " 2011 IEEE Symposium on Industrial Electronics and Applications pp. 100-103.

[88] L. Yang and G. B. Giannakis, (2004), "Ultra-Wideband Communications An Idea Whose Time Has Come," IEEE Signal Processing Magazine, November pp. 26-54.

[89] C. Y. Lee and C. Toumazou, (2005), "Ultra-low Power UWB for Real Time Biomedical Wireless Sensing," *IEEE International Symposium on Circuits and Systems*, vol. 1 23-26 May, pp. 57-60.

[90] H. P. Koringa, B. H. Joshi and Dr. V. A. Shah, (2015), "High Power Gain Low Noise Amplifier Design for Next Generation 1-7GHz Wideband RF Frontend RFIC using 0.18µm CMOS" *in IEEE 19th International Symposium on VLSI Design and Test (VDAT-2015),*26-29 June.

[91] H. P. Koringa and Dr. V. A. Shah, (2016), "Ultra Wideband Low Noise Amplifier Design and Optimization for Next Generation RF Receiver using 0.18µm CMOS" *in 3rd International Conference on Microelectronics, Circuits & Systems (Micro2016),* 9-10 July, pp. 70-76.

[92] H. P. Koringa, Dr. V. A. Shah and Dr. M. V. Shah, (2016), "Highly Linear Active feedback noise cancelling Wideband Low Noise Amplifier for Next Generation RF Frontend using 0.18um CMOS" in IJAREST International journal vol. 3, (1) pp.148-155.

List of Bibliography

[1] A. Abidi, (1986), "High-frequency noise measurements on FET's with small dimensions", IEEE Trans. Electron Devices, vol. 33 (11) pp. 1801–1805.

[2] Abidi, (2007), "The path to the software-defined radio receiver", IEEE J. Solid State Circuits, vol. 42 (5).

[3] B. Razavi, (2006), "Design of a 60 GHz RF frontend", IEEE J. Solid State Circuits 41 (1) pp.17–21.

[4] C. Svensson and J. J. Wikner, (2010), "Power consumption of analog circuits: a tutorial", Analog Integrated Circuits and Signal Processing, vol. 65 pp. 171–184.

[5] C. Toumazou, G. S. Moschytz and B. Gilbert, (2004), "Trade-offs in Analog Circuit Design" The Designer's Companion, Part1, Springer.

[6] G. Sapone and G. Palmisano, (2011), "A 3–10GHz low-power CMOS low-noise amplifier for ultra-wideband communication", IEEE Trans. Microwave Theory Tech., vol. 59 (3).

[7] H. Doh, Y. Jeong, S. Jung, and Y. Joo, (2004), "Design of CMOS UWB low noise amplifier with cascode feedback", *47th IEEE International Midwest Symposium on Circuits and systems*.

[8] H. T. Ahn, and D. J. Allstot, (2002), "0.5-8.5 GHz fully differential CMOS distributed amplifier", IEEE Journal of Solid-State Circuits, vol. 37 (8) pp. 985 – 993.

[9] L. E. Larson (1998), "Integrated circuit technology options for RFICs—present status and future directions", IEEE J. Solid State Circuits, vol. 33 (3).

[10] Po Yu Chang and Shawn S. H. Hsu, (2010), "A compact 0.1–14GHz ultra-wideband low noise amplifier in 0.13-mm CMOS, IEEE Trans. Microwave Theory Tech., vol. 58 (10).

[11] R. Ludwig and P Bretchko, (2000), "RF Circuit Design", Prentice Hall.

[12] R. Roovers, D. M. W. Leenaerts, J. Bergervoet, K. S. Harish, R. C. H. Beek and G. Weide, (2005), "An interference robust receiver for ultra-wideband radio in SiGe BiCMOS technology", IEEE J. Solid-State Circuits, vol. 40 (12) pp. 2563-2572.

[13] Reza Molavi, (2005), "Design of Wideband CMOS Low Noise Amplifiers", Master Thesis of University of British Columbia.

[14] S. Arshad, F. Zafar, R. Ramzan, and Q. Wahab, (2013), "Wideband and multiband CMOS LNA As: State of the art and future prospects", Elsevier Microelectronics Journal.

[15] S. Vishwakarma, J. Sungyong, and J. Youngjoong, (2004), "Ultra Wideband CMOS Low Noise Amplifier with Active Input Matching", *International Workshop on Ultra Wideband Systems, 2004. Joint with Conference on Ultra wideband Systems and Technologies. Joint UWBST & IWUWBS*, 18-21 May pp. 415 – 419.

[16] V. Aparin, P. Gazzerro, J. Zhou, B. Sun, S. Szabo, and E. Zeisel, (2002), "A highly integrated tri-band/quad-mode SiGe BiCMOS RF-to-baseband receiver for wireless CDMA/ WBCDMA/ AMPS applications with gps capability", *IEEE International Solid-State Circuits Conference Digest of Technical Papers.*

[17] W. Zhuo, (2005), "A capacitor cross-coupled common gate low-noise amplifier", IEEE Trans. Circuits System II, Exp. Briefs, vol. 52 (12) pp. 875–879.

List of Publications

Papers Published

1) Hasmukh P Koringa, Dr. Vipul A Shah and Prof. Durga Misra, (2013) "Estimation and Optimization of Power dissipation in CMOS VLSI circuit design: A Review Paper" in IJETEE Journal, vol. 1, pp. 14-21, ISSN No. 2320-9569.

2) Hasmukh P Koringa, Bhusan D Joshi and Dr. Vipul A Shah, (2015) "High Power Gain Low Noise Amplifier Design for Next Generation 1-7GHz Wideband RF Frontend RFIC using 0.18µm CMOS" *in proceeding of IEEE 19th International Symposium on VLSI Design and Test (VDAT-2015)* 26-29 June, pp. 420-424. IEEE Explore DOI 10.1109/ISVDAT.2015.7208105.

3) Hasmukh P Koringa and Dr. Vipul A Shah, (2015) "Design and Optimization of Narrow Band Low Noise Amplifier using 0.18µm CMOS" *in proceeding of IEEE international conference of communication and networking 2015,* 19-21 Nov., pp. 100-106. IEEE Explore DOI 10.1109/ICCN.2015.21.

4) Hasmukh P Koringa and Dr. Vipul A Shah, (2016) "Wideband Low Noise Amplifier for Next Generation Wireless RF Frontend: A Review Paper" in IJAREST International journal, vol. 3, issue 1, pp. 116-125. e-ISSN No.: 2393-9877, p-ISSN No.: 2394-2444.

5) Hasmukh P Koringa, Dr. Vipul A Shah and Dr. Mihir V Shah, (2016) "Highly Linear Active feedback noise cancelling Wideband Low Noise Amplifier for Next Generation RF Frontend using 0.18um CMOS" in IJAREST International journal, vol. 3, issue 1, pp. 148-155. e-ISSN No.: 2393-9877, p-ISSN No.: 2394-2444.

6) Hasmukh P Koringa, and Dr. Vipul A Shah, (2016) "Ultra Wideband Low Noise Amplifier Design and Optimization for Next Generation RF Receiver using 0.18µm CMOS" *in proceeding of 3rd International Conference on Microelectronics, Circuits & Systems (Micro2016),* 9-10 June, pp. 70-76.

Paper Submitted

7) Hasmukh P Koringa and Dr. Vipul A Shah, (2016), "Ultra Wideband Low Noise Amplifier Design and Optimization for Next Generation RF Receiver using 0.18µm CMOS", Communications on Applied Electronics (CAE) international Journal, Foundation of Computer Science FCS, New York, USA.