**GUJARAT TECHNOLOGICAL UNIVERSITY, AHMEDABAD, GUJARAT**

**Course Curriculum**

**DIGITAL TECHNIQUES**
**(Code: 3331703)**

| Diploma Programme in which this course is offered | Semester in which offered |
|---|---|
| Instrumentation and Control Engineering | 3rd semester |

## 1. RATIONALE

Digital electronics and techniques are almost part and parcel of any modern industrial equipment. Integrating industrial process signals for logical and mathematical operations, using combinational and sequential logic for process control components are some of the skills required in this area by IC engineers. This requires every diploma engineer to possess the basic skills of digital techniques to maintain various digitally controlled industrial process systems effectively and efficiently. Hence, this course has been designed to fulfill this purpose.

## 2. COMPETENCY ('Programme Outcome' according to NBA Terminology)

The course content should be taught and implemented with the aim to develop different types of skills so that students are able to acquire following competency:

- **Maintain various industrial process control systems which are digitally controlled.**

## 3. TEACHING AND EXAMINATION SCHEME

| Teaching Scheme (In Hours) | | | Total Credits (L+T+P) | Examination Scheme | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | Theory Marks | | Practical Marks | | Total Marks |
| L | T | P | C | ESE | PA | ESE | PA | |
| 4 | 0 | 2 | 6 | 70 | 30 | 20 | 30 | **150** |

**Legends: L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** - Practical; **C** - Credit; **ESE** - End Semester Examination; **PA** - Progressive Assessment

## 4. COURSE DETAILS

| Unit | Major Learning Outcomes ('Course Outcomes' in Cognitive Domain according to NBA terminology) | Topics and Sub-topics |
|---|---|---|
| **Unit – I Number Systems** | 1a. Represent given number in the other given number system. | 1.1 Number systems: Decimal, Binary, Octal and Hexadecimal |
| | 1b. Perform arithmetic operations on binary numbers. | 1.2 Binary arithmetic Operation: addition, subtraction, multiplication and division |
| | 1c. Obtain 1's and 2's compliment of given binary number.<br>1d. Subtract given binary numbers using 1's and 2's compliment method. | 1.3 Compliments: 1's and 2's compliments, subtraction by 1's and 2's compliment method |
| | 1c. Convert the given number from one number system to another number system. | 1.4 Conversion: Binary to decimal, octal, hexadecimal conversion and vice versa. Octal to decimal, hexadecimal, binary conversion and vice-versa, hexadecimal to octal, decimal, Binary and vice versa. |
| **Unit – II Logic Gates and Boolean Algebra** | 2a. Select electrical levels for '0' and '1' on and off Low and High logical operation.<br>2b. Differentiate between positive and negative logic system.<br>2c. State tri-state operation. | 2.1 Two state operation<br>2.2 Positive and negative logic system<br>2.3 Tristate logic operation |
| | 2d. Draw the symbol and equivalent electrical circuits of given gates.<br>2e. Explain functionality of any gate with the help of its truth table .<br>2f. Implement basic gates and other gates with the help of universal gate. | 2.4 Basic gates : AND,OR, NOT Gate, universal gates: NAND and NOR, other gates:EX-OR, EX-NOR Equivalent electrical circuits, truth table and functional operation of each gates |
| | 2g. State and verify First and Second De Morgan's theorem. | 2.5 De Morgan's theorems |
| | 2h. State Theorems of Boolean algebra. | 2.6 Laws, theorems and postulates of Boolean algebra |
| | 2i. Simplify the given expression using Boolean algebra and Karnaugh map method (up to 4 variables).<br>2j. Realise logic circuits of the simplified expression using truth table and AND-OR/ OR-AND/ NAND-NAND logic gates. | 2.7 Boolean expression: Sum of products and product of sums<br>2.8 Karnaugh map method for simplification of Boolean expression |

| Unit | Major Learning Outcomes ('Course Outcomes' in Cognitive Domain according to NBA terminology) | Topics and Sub-topics |
|---|---|---|
| **Unit – III Combinational Logic Circuits** | 3a. Define combinational logic circuit.<br>3b. Test the logic circuits with the help of truth table. | 3.1 Combinational logic circuit.<br>3.2 Arithmetic Circuits: Half adder, full adder, half and full subtractor, 1's and 2's compliment subtractor circuit, 2's compliment subtractor/adder circuit. |
| | 3c. Convert given numbers from binary to Gray and Gray to binary codes. | 3.3 Code Converters: Binary to gray and gray to binary code converters ( up to 4 bit ). |
| | 3d. Explain working of various given combinational circuits with logic diagram and truth table.<br>3e. List IC numbers of given combinational circuits. | 3.4 Decoder (3 to 8), Encoder circuits ( 8 to 3).<br>3.5 Parity bit Generators and Checker circuits.<br>3.6 Multiplexer (4:1line), Demultiplexers (1:4 line). |
| **Unit – IV Sequential Logic Circuits** | 4a. Define terms related to sequential logic circuits. | 4.1 Digital clock signal, clock skew, duty cycle, synchronous and asynchronous circuit operation, Edge and Level triggered operation. |
| | 4b. Differentiate between combinational and sequential circuit.<br>4c. Explain the truth tables of the given Flip flops.<br>4d. List the applications of Flip-Flop. | 4.2 Flip-Flops: S-R, J-K, T and D. Truth table and logic circuits of each flip-flop |
| | 4e. Define register and shift register.<br>4f. Describe with sketches the data movement in shift registers.<br>4g. List the applications of shift register in digital instruments. | 4.3 Shift Registers: Series and parallel, shift, Serial in serial out, Shift Register. |
| | 4h. List various counters.<br>4i. Explain the function of ripple counter (implemented using JK Flip flops) with the help of truth table. | 4.4 Counters: Ripple counter, Mod counter, up – down counter, synchronous and asynchronous counters |
| | 4j. Classify types of conversions.<br>4k. List applications of A/D and D/A Conversion in instrumentation<br>4l. Describe the block diagram of sensing motion. | 4.5 A/D and D/A Converter<br>4.6 Digital Clock |

| Unit | Major Learning Outcomes ('Course Outcomes' in Cognitive Domain according to NBA terminology) | Topics and Sub-topics |
|---|---|---|
| | 4m. Describe with block diagram working of a digital clock. | |
| **Unit – V Control and Interfacing of process parameters** | 5a. Develop logic signals ( 0 and 1)<br>5b. Sketch the logic circuit for logical operations | 5.1. Process Logic components for *level control* loop: Level Switch configuration: HL, HH, HHL, HHH, LL, LLL and LLH. |
| | 5c. Develop logic signals ( 0 and 1)<br>5d. Sketch the logic circuit for logical and mathematical operations. | 5.2. Process Logic components for *Temperature control* loop: Temperature Switch configuration: HL, HH, HHL, HHH, LL, LLL and LLH. |
| | 5e. Develop logic signals ( 0 and 1)<br>5f. Sketch the logic circuit for logical operations | 5.3. Process Logic components for *Pressure control* loop: Pressure Switch configuration: HL, HH, HHL, HHH, LL, LLL and LLH. |
| | 5g. Develop logic signals ( 0 and 1)<br>5h. Sketch the logic circuit for logical and mathematical operations. | 5.4. Process Logic components for *flow control* loop: Flow Switch configuration: HL, HH, HHL, HHH, LL, LLL and LLH. |
| | 5i. Develop logic signals ( 0 and 1)<br>5j. Sketch the logic circuit ircuit for logical operations | 5.5. Process Logic components for *Speed control* loop: Speed Switch configuration: HL, HH, HHL, HHH, LL, LLL and LLH. |

## 5. SUGGESTED SPECIFICATION TABLE WITH HOURS and MARKS (THEORY)

| Unit | Unit Title | Teaching Hours | Distribution of Theory Marks | | | |
|---|---|---|---|---|---|---|
| | | | R Level | U Level | A Level | Total Marks |
| I | Number Systems | 12 | 04 | 08 | 02 | 14 |
| II | Logic Gates and Boolean Algebra | 12 | 04 | 04 | 06 | 14 |
| III | Combinational Logic Circuits | 12 | 02 | 04 | 08 | 14 |
| IV | Sequential Logic Circuits | 08 | 02 | 02 | 03 | 07 |
| V | Control and Interfacing of process parameters | 12 | 03 | 06 | 12 | 21 |
| **Total** | | **56** | **15** | **24** | **31** | **70** |

**Legends:** R = Remember; U = Understand; A = Apply and above levels (Bloom's revised taxonomy)

**Note:** This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

## 6. SUGGESTED LIST OF EXERCISES/PRACTICALS

The practical/exercises should be properly designed and implemented with an attempt to develop different types of practical skills **(Course Outcomes in psychomotor and affective domain)** so that students are able to acquire the competencies (Programme Outcomes). Following is the list of practical exercises for guidance.

**Note**: Here only course outcomes in psychomotor domain are listed as practical/exercises. However, if these practical/exercises are completed appropriately, they would also lead to development of Programme Outcomes/Course Outcomes in ***affective domain*** as given in a common list at the beginning of curriculum document for this programme. Faculty should refer to that common list and should ensure that students also acquire those Programme Outcomes/Course Outcomes related to affective domain.

| S. No. | Unit No. | Practical/Exercise ('Course Outcomes' in Psychomotor Domain according to NBA terminology) | Apprx. Hrs. Required |
|---|---|---|---|
| 1. | II | Test the functionality of basic logic gates. | 2 |
| 2. | II | Build/ test the functionality of exclusive-OR gate. | 2 |
| 3. | II | Build/test the functionality of NAND gate as a universal logic gate. | 2 |
| 4. | II | Build/test the functionality of NOR gate as a universal logic gate . | 2 |
| 5. | III | Build/test the HALF ADDER circuit. | 2 |
| 6. | III | Build/test the FULL ADDER circuit. | 2 |
| 7. | III | Build/test HALF SUBTRACTOR circuit. | 2 |
| 8. | III | Check the functionality of parity /generator checker circuit. | 2 |
| 9. | IV | Build/ Test the Ripple counter(Four bit). | 2 |
| 10. | IV | Check the performance of SEVEN SEGMENT display. | 2 |
| 11. | IV | Build/ Test the functionality of SR flip-flop. | 2 |
| 12. | IV | Build/ Test the functionality of JK flip-flop. | 2 |
| 13. | IV | Build/ Test the shift register. | 2 |
| 14. | IV | Determine the digital output for the given analog input signal through analog to digital converter circuit. | 2 |
| 15. | IV | Determine the analog output for the given digital input the digital to analog converter circuit. | 2 |
| 16. | V | Build/ Test AND, OR, EX-OR Logic circuits for temperature loop. | 2 |
| 17. | V | Build/ Test AND,OR,EX-OR Logic for level loop. | 2 |
| 18. | V | Build/ Test NAND,NOR Logic for temperature loop. | 2 |
| 19. | V | Build/ Test NAND,NOR Logic for level loop. | 2 |
| 20. | V | Build/ Test AND,OR,EX-OR Logic for flow loop. | 2 |
| 21. | V | Build/ Test NAND,NOR Logic for flow loop. | 2 |
| | **Total** | | **42** |

## 7. SUGGESTED LIST OF STUDENT ACTIVITIES

Following is the list of proposed student activities such as:

i. Students may be asked to collect photographs using internet which is relevant to field application of various topics and have to prepare learning materials using it.
ii. Teachers guided self learning activities, Course/library/internet/lab based mini projects, industrial visit etc.
iii. Students activities like: course/ topic based seminars, Internet based assignments.
iv. Students should deliver a seminar in groups on materials used in various Digital Techniques and advances/latest trends in Digital Techniques.

## 8. SPECIAL INSTRUCTIONAL STRATEGIES (if any)

i. Take small instrumentation components to the class when teaching
ii. Give simple numerical to students on Boolean Algebra
iii. Internet based home assignments
iv. Mini project

## 9. SUGGESTED LEARNING RESOURCES

### A) List of Books:

| S. No. | Title of Books | Author | Publication |
|---|---|---|---|
| 1 | Digital circuit | Kumar, Ananad | PHI Learning, New Delhi , Latest edition |
| 2 | Digital Electronics | Kharate, G.K. | Oxford University Press, Latest edition |
| 3 | Principles of digital electronics | Malvino and Leach | TMH, New Delhi , Latest edition |
| 4 | Digital Design | Mano ,M. Morris | Pearson, New Delhi , Latest edition |
| 5 | Digital electronics :Principles, devices and applications | Maini ,A .K. | John Willy and Sons, Latest edition |
| 6 | Digital Techniques | Godse ,A.P. | Technical publications, Latest edition |
| 7 | Applied Instrumentation in the Process Industries | William G. Andrews | Gulf Publication, London, Latest edition |

### B) List of Major Equipment/Materials with Broad Specifications

i. Bread boards
ii. DC Regulated power supply 0-30 volt DC (10 Nos.)
iii. Digital IC Tester (40 pins)
iv. Digital Logic trainer kit (10 Nos.)
v. Hardwired relay logic trainer (5 Nos.)
vi. Digital level switch, temperature switch, flow switch with logics HL, HH, HHL, HHH, LL, LLL and LLH.

### C) List of Software/Learning Websites

i. www.nptel.com
ii. http://en.wikipedia.org/wiki/Digital_electronics
iii. http://my.safaribooksonline.com/book/electrical-engineering/computer-engineering/9780750645829/chapter-10dot-instrumentation-and-interfacing/
iv. http://www.hss.energy.gov/deprep/ftcp/directives/QSR-InstrumentationControl.pdf

## 10. COURSE CURRICULUM DEVELOPMENT COMMITTEE

**Faculty Members from Polytechnics**

- **Prof. R. R. Manchiganti**, HOD IC Engineering, Govt. Polytechnic, Gandhinagar
- **Prof. M.V. Dabhi**, Lecturer IC Engineering, Government Polytechnic Gandhinagar
- **Prof. R.D. Sathwara**, Lecturer IC Engineering, Govt. Polytechnic. Gandhinagar
- **Prof. A.M. Patel,** Lecturer IC Engineering, Government Polytechnic, Palanpur

**Faculty Members from NITTTR_Bhopal**

- **Dr. Anjali Potnis**, Associate Professor, Department of Electrical and Electronics Engineering.
- **Dr. Joshua Earnest**, Professor, Department of Electrical and Electronics Engineering.