GUJARAT TECHNOLOGICAL UNIVERSITY, AHMEDABAD, GUJARAT

Course Curriculum

DIGITAL CIRCUITS
(Code: 3332002)

Diploma Programme in which this course is offered	Semester in which offered
Mechatronics Engineering	3rd Semester

1. RATIONALE

In the area of Mechatronics, a digital electronic circuit is an inseparable part. Hence every mechatronic diploma engineer needs to have the basic skills of maintaining the digital circuits which are part of the mechatronic equipment. Therefore, this course contains contents related to number system, logic gates, Boolean implementation, basic combinational logic and sequential circuits. Hence, by studying this course the student will be able to maintain digital circuits in mechatronic equipment.

2. COMPETENCY (Programme Outcome according to NBA Terminology)

The course content should be taught and implemented with the aim to develop different types of skills leading to the achievement of the following competencies:

- **Maintain digital circuits in mechatronic equipment.**

3. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	ESE	PA	ESE	PA	
4	0	2	6	70	30	20	30	150

Legends: L - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** - Practical; **C** - Credit; **ESE** - End Semester Examination; **PA** - Progressive Assessment

4. COURSE DETAILS

Unit	Major Learning Outcomes (Course Outcomes in Cognitive Domain according to NBA terminology)	Topics and Sub-topics
Unit – I Number System and Binary Codes	1a. Convert number systems and its complements 1b. Solve problems number systems and binary codes	1.1 Numbers system: Base Conversion of Decimal, Binary, Octal, Hexadecimal 1.2 Complement Methods: 1's and 2's complement 1.3 Binary Codes : BCD code, Excess-3 code, Gray code, Parity code
Unit – II Logic Gates	2a. Describe functions of Binary Logic 2b. Differentiate the functions of Basic Logic Gates and Universal Logic Gates 2c. Explain the Truth table of various logic gates	2.1 Positive and Negative Logic 2.2 Basic Logic Gates: AND, OR , NOT gate 2.3 Derived Logic Gates: EX-OR, EX-NOR 2.4 Implementation using Basic Gates 2.5 Universal Logic Gates: NAND, NOR gate 2.6 Implementation using NAND and NOR gate
Unit – III Boolean Function Implementation	3a. Simplify the Boolean function using Boolean theorems and Boolean Algebra 3b. Differentiate between SOP and POS 3c. Simplify Boolean function using K-map	3.1 Boolean Function:Laws of Boolean Algebra,De-Morgan's Theorems, Sum of Product (SOP) Form, Product of Sum (POS) Form, Minterms and Maxterms 3.2 Simplification of Boolean Function using 3.3 Boolean Algebra 3.4 Simplification of Boolean Function using 3.5 K-map: Up to four Variable, Don't Care Condition
Unit – IV Combinational Circuits	4a. Modify half adder, full adder, half Subtractor and full Subtractor 4b. List Applications of multiplexers and Demultiplexers 4c. Differentiate between octal to binary encoders . 4d. Explain the working of a BCD to 7-segment Decoders.	4.1. Adder : Half Adder, Full Adder 4.2. Subtractor : Half and Full Subtractor 4.3. 2-bit Magnitude Comparator 4.4. Multiplexer and Demultiplexer: Multiplexer (4:1), Demultiplexer (1:4) 4.5. Encoder and Decoder: Octal to Binary Encoder (8:3), Decoder (3:8), BCD to 7-segment Decoder
Unit – V Sequential Circuits	5a. Design clocked Flip Flops using S-R Latch 5b. Explain the working of shift left and shift right register 5c. Distinguish between 4-bit ripple counter, decade counter and UP/DOWN counters	5.1 S-R Latch: NOR Latch, NAND Latch 5.2 Clocked Flip Flops: S-R, J-K, T and D Flip- Flop 5.3 Applications of Flip Flops 5.4 Shift Register : Series and Parallel Shift, Left and Right Shift 5.5 Counters:4-bit Binary Ripple Counter, Modulo Counters (Mod-6, Mod-10),4-bit synchronous UP/DOWN Counters

5. SUGGESTED SPECIFICATION TABLE WITH HOURS and MARKS (THEORY)

Unit	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Number System and Binary Codes	12	6	6	2	14
II	Logic Gates	08	6	6	2	14
III	Boolean Function Implementation	12	4	4	6	14
IV	Combinational Circuits	12	2	4	8	14
V	Sequential, Circuits	12	2	4	8	14
Total		**56**	**20**	**24**	**26**	**70**

6. SUGGESTED LIST OF EXERCISES/PRACTICALS

The practical/exercises should be properly designed and implemented with an attempt to develop different types of practical skills (**Course Outcomes in psychomotor and affective domain)** so that students are able to acquire the competencies (Programme Outcomes). Following is the list of practical exercises for guidance.

Note: Here only course outcomes in psychomotor domain are listed as practical/exercises. However, if these practical/exercises are completed appropriately, they would also lead to development of **Programme Outcomes/Course Outcomes in *affective domain*** as given in a common list at the beginning of curriculum document for this programme. Faculty should refer to that common list and should ensure that students also acquire those Programme Outcomes/Course Outcomes related to affective domain.

S. No.	Unit No.	Practical/Exercise (Course Outcomes in Psychomotor Domain according to NBA terminology)	Approx. Hrs. Required
1	I	Convert decimal number system to binary, octal and hex. Convert binary, octal and hex to decimal.	02
2	I	Convert octal to hex and hex to octal number.	01
3	I	Convert binary to BCD, Excess-3 and gray code Convert BCD, Excess-3 and gray code to binary	01
4	II	Test the functionality of the AND gate using IC 7408, OR gate using IC 7432 and NOT gate using IC 7404.	02
5	II	Test the functionality of the EX-OR gate using IC 7486 and EX-NOR gate using IC 74266.	01
6	II	Implement Boolean expression using basic logic gates	01
7	II	Test the functionality of the NAND gate using IC 7400 and NOR gate using IC 7402.	02
8	II	Test the functionality of NAND gate (IC 7400) as a universal building block.	02
9	II	Test the functionality of NOR gate (IC 7402) as a universal building block.	02
10	IV	Design and implement Half Adder and full adder circuit using IC 7486, 7408 and 7404.	02
11	IV	Design and implement Half Subtractor and full Subtractor circuit using IC 7486, 7408 and 7404.	02
12	IV	Design and implement 2-bit magnitude comparator using basic logic gates	02

S. No.	Unit No.	Practical/Exercise (Course Outcomes in Psychomotor Domain according to NBA terminology)	Approx. Hrs. Required
13	IV	Build and Test 4:1 Multiplexer (IC 74153) and 1:4 Demultiplexer (IC 74155) circuit	02
14	IV	Realize octal to binary encoder circuit using IC 74148	02
15	IV	Realize BCD to 7-segment decoder circuit using IC 7447	02
16	V	Realize Clocked S-R Flip Flop and clocked D Flip Flop	02
17	V	Realize Clocked T Flip Flop and clocked J-K Flip Flop	02
18	V	Implement 8-bit shift register using IC 74198.	02
19	V	Implement 4-bit binary counter using IC 74293.	02
20	V	Implement decade counter using IC 74290.	02
21	V	Implement synchronous UP/DOWN decade counter using IC 74168.	02
	Total		**40**

*Note: Minimum 12 experiments should be performed and at least two to three Experiments selected from each unit.

7. SUGGESTED LIST OF STUDENT ACTIVITIES

Following is the list of proposed student activities like:

i. Course/Topic based seminars,
ii. internet based assignments,
iii. teacher guided self learning activities,
iv. course/library/internet/lab based mini-projects etc. These could be individual or group-based. Students can refer datasheet or data manuals to study the pin diagram of various digital ICs.

8. SPECIAL INSTRUCTIONAL STRATEGIES (if any)

i. Learning Digital Circuits in the class room takes place through activities like Seminar, group's discussion, Assignments and project.
ii. Preparing notes for laboratory work, design circuit and truth tables in the class room before the practical work in the laboratory.

Guidelines for Progressive Assessment (PA) of Theory

The Progressive Assessment of theory may include the few activities like: Class Test, Assignment, Seminar/Symposium on application of digital circuits, Project, Collection/ Records of IC datasheet, Group discussion/Debate

Guidelines for Progressive Assessment (PA) of Practical

Distribution of Marks for different Components in Progressive Assessment (PA)		
S. No	**Content**	**% of Marks**
1	Lab Record.	25%
2	Performing of the practical/exercise	25%
3	Viva voice.	20%
4	Planning, team working, communication etc.	15%
5	Timely Submission, Punctuality and Attendance.	15%
Total		**100%**

9. SUGGESTED LEARNING RESOURCES

A) List of Books

S. No.	Title of Books	Author	Publication
1	Fundamentals of Digital Circuits	A. Anand Kumar	PHI Learning, Latest Edition ISBN**:** 81-203-1745-9
2	Digital Logic and Computer Design	Mano M. Morris	Pearson publication, Latest Edition ISBN**:** 81-203-0417-9
3	Digital Electronics Principles	Malvino and Leech	Tata McGraw-Hill, New Delhi, Latest Edition

B) List of Major Equipment/Materials with Broad Specifications

i. Breadboard
ii. Function Generator
iii. Digital Multi Meter (DMM)
iv. Cathode Ray Oscilloscope (CRO)
v. DC Power supplies
vi. Experimental Boards

C) List of Software/Learning Websites

i. Practical Semiconductor Data Manuals: BPB Publications; New Delhi
ii. Magazines like Electronics for you.
iii. Electronic Work Bench, MultiSIM
iv. www.alldatasheet.com
v. http://www.asic-world.com/digital/tutorial.html
vi. www.nptel.com

10. COURSE CURRICULUM DEVELOPMENT COMMITTEE

Faculty Members from Polytechnics

- **Prof. H. A. Momaya**, Senior Lecturer, Electronics and Communication Department, B. S. Patel Polytechnic, Kherva, Mehsana.
- **Prof. P. A. Solanki,** Senior Lecturer, Mechatronics Department, B. S. Patel Polytechnic, Kherva, Mehsana.
- **Prof. K. P. Patel**, Head of Department, Mechatronics Department, B. S. Patel Polytechnic, Kherva, Mehsana.

Faculty Members from NITTTR, Bhopal

- **Prof. A.S. Walkey,** Associate professor Department of Electrical and Electronics Engineering
- **Dr. Anjali Potnis,** Assistant Professor, Department of Electrical and Electronics Engineering.