

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER– IV(NEW) EXAMINATION – SUMMER 2023****Subject Code:2140707****Date:17-07-2023****Subject Name:Computer Organization****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

MARKS

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|------------|---|-----------|
| Q.1 | (a) List and briefly explain the functionalities of components of CPU. | 03 |
| | (b) Discuss the following addressing modes with example(s):
- immediate
- relative | 04 |
| | (c) Draw and explain flowchart for instruction cycle without interrupt in detail. | 07 |
| Q.2 | (a) Write differences between register stack and memory stack. | 03 |
| | (b) Briefly explain hardwired control unit of basic computer. | 04 |
| | (c) Draw and explain hardware implementation of Binary Adder-Subtractor. | 07 |
| | OR | |
| | (c) Write a program to evaluate the following arithmetic statement
$Z = A - (B * C) + D * (E / F)$
1. using a general register computer with three-address instructions,
2. using an accumulator type computer with one-address instructions,
3. using a stack organized computer with zero-address instructions. | 07 |
| Q.3 | (a) Define the following terms:
- microoperation
- microinstruction
- microprogram | 03 |
| | (b) Write assembly language program which adds two numbers. Write assumptions if any/required. | 04 |
| | (c) Write a detailed note on general register organization. | 07 |
| | OR | |
| Q.3 | (a) Write differences between hardwired control and microprogrammed control organization. | 03 |
| | (b) Explain status bit conditions with neat sketches. | 04 |
| | (c) Discuss pipeline conflicts with their proposed solution(s). | 07 |
| Q.4 | (a) Explain 2-bit by 2-bit array multiplier. | 03 |
| | (b) Convert the following arithmetic expression into prefix and postfix notation.
$(A * B) - C + (D / E + F * G)$ | 04 |
| | (c) Describe arithmetic pipeline with neat sketches. | 07 |
| | OR | |
| Q.4 | (a) Write differences between RAM and ROM. | 03 |

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| | (b) | Illustrate the CPU-IOP communication with the help of flow chart in brief. | 04 |
| | (c) | Draw flowchart for Booth algorithm and explain the same by taking an appropriate example. | 07 |
| Q.5 | (a) | State the differences between tightly coupled multiprocessors and loosely coupled multiprocessors. | 03 |
| | (b) | Briefly discuss on memory hierarchy. | 04 |
| | (c) | Describe DMA with suitable block diagram. Explain why does DMA have priority over the CPU when both request a memory transfer? | 07 |
| | | OR | |
| Q.5 | (a) | State the differences between RISC and CISC. | 03 |
| | (b) | Briefly discuss cache coherence problem and also suggest its proposed solution(s). | 04 |
| | (c) | Explain the following with respect to cache memory: | 07 |
| | | - Associative mapping | |
| | | - Set-associative mapping | |
