

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER-VI (NEW) EXAMINATION – SUMMER 2023****Subject Code:2161101****Date:12-07-2023****Subject Name:VLSI Technology & Design****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

		MARKS
Q.1	(a) What is the difference between positive photo resist and negative photo resist? Which is commonly used in the manufacturing of high density integrated circuits?	03
	(b) Discuss following approaches (with examples) used to reduce complexity of IC design: 1. Hierarchy, 2. Regularity, 3. Modularity, and 4. Locality.	04
	(c) Draw and explain various fabrication steps for CMOS inverter with proper notations at each fabrication steps.	07
Q.2	(a) Compare: Semi-custom and Full custom VLSI design style.	03
	(b) Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA)	04
	(c) Calculate the threshold voltage V_{TO} at $V_{SB}=0$, for silicon gate n channel MOS transistor, with the following parameters: substrate doping density $N_A=3 \times 10^{17} \text{ cm}^{-3}$, $N_D = 4 \times 10^{19} \text{ cm}^{-3}$, $\Phi_{F(gate)} = 0.58\text{V}$, gate oxide thickness $t_{ox} = 200\text{\AA}$, and oxide interface fixed charge density $N_{ox} = 10^{10} \text{ cm}^{-2}$. Consider Boltzmann Constant = $1.38 \times 10^{-23} \text{ (J/K)}$, Electron charge = $1.6 \times 10^{-19} \text{ C}$, Intrinsic Silicon carrier concentration = $1.45 \times 10^{10} \text{ cm}^{-3}$, $\epsilon_{Si} = 11.7\epsilon_0$ and $\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$, $\epsilon_{ox} = 3.97\epsilon_0 \text{ F/cm}$.	07
	OR	
	(c) For an enhancement type NMOS transistor $V_T = 0.8 \text{ V}$, $\lambda = 0.04 \text{ 1/V}$, $\mu_n * C_{ox} = 20 \text{ A/V}^2$, $W/L = 20 \mu\text{m}$, $V_G = 5 \text{ V}$, $V_D = 4 \text{ V}$, $V_S = 2 \text{ V}$. Calculate Drain Current I_D .	07
	Physical constants : Thermal voltage $= kT/q = 0.026 \text{ volt}$. Energy Gap of silicon (Si) $= E_g = 1.12 \text{ eV}$. Intrinsic Carrier Concentration of silicon $= n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$. Dielectric constant of vacuum $= \epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$. Dielectric constant of silicon $= \epsilon_{Si} = 11.7 \times \epsilon_0 \text{ F/cm}$. Dielectric constant of silicon dioxide $= \epsilon_{ox} = 3.97 \times \epsilon_0 \text{ F/cm}$	
Q.3	(a) Draw CMOS inverter. Explain its voltage transfer characteristic. Also explain the NM_L and NM_H noise margins with respect to this transfer characteristic	03
	(b) Define propagation delay and derive the expression for τ_{PHL} for CMOS inverter. Assume ideal step as an input to CMOS inverter.	04
	(c) Consider a resistiveload inverter circuit with $V_{DD} = 5 \text{ V}$, $K_n' = 10 \mu\text{A/V}^2$, $V_{TO} = 0.8 \text{ V}$, $R_L = 400 \text{ k}\Omega$ and $W/L = 2$. Calculate the critical Voltages (V_{OH} , V_{OL} , V_{IL} and V_{IH}) on the VTC and find the noise margins of the circuit.	07

OR

- Q.3** (a) What is meant by static and dynamic power dissipation? **03**
 (b) Draw resistive load inverter. Derive V_{IL} and V_{IH} critical voltage equation of resistive load inverter. **04**
 (c) Consider a CMOS inverter with the following parameters: **07**
 $V_{DD}=3.3\text{ V}$, $V_{T0,n}=0.6\text{ V}$, $V_{T0,p}=-0.7\text{ V}$, $k_n=200\text{ }\mu\text{A/V}^2$ and $k_p=80\text{ }\mu\text{A/V}^2$
 Calculate the noise margins of the circuit. Consider $kR=2.5\text{ V}$ and $V_{T0,n}\neq|V_{T0,p}|$ as it is not a symmetric CMOS inverter.
- Q.4** (a) The pass transistor followed by inverter is shown below in Figure 1. Find the output voltage. Also find intermediate stage voltages like V_x , V_y and V_z . **03**
 $V_A=5\text{V}$, $V_B=V_C=V_D=3.5\text{V}$

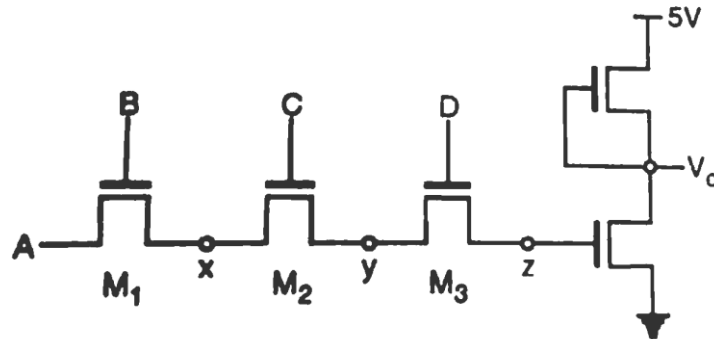


Figure 1

- (b) What are the limitations of Dynamic circuits? Discuss the effect of charge sharing and charge leakage in dynamic pass transistor logic. **04**
 (c) Explain the Euler path approach to find the optimized stick-diagram for any CMOS logic circuit. Draw the optimized stick-diagram for the following Boolean function (CMOS Logic), $F=(A(D+E)+BC)'$. Explain the importance of Euler path approach. **07**
- OR**
- Q.4** (a) Explain Pass Transistor logic (PTL) and Complementary Pass Transistor logic (CPTL). Implement EX-OR/EX-NOR Gate using CPTL. **03**
 (b) Explain the need of Voltage bootstrapping? Derive the mathematical expression for dynamic Voltage bootstrapping circuit. **04**
 (c) For the Exclusive OR function, draw with following realization **07**
 1. Static CMOS realization
 2. Pseudo nMOS gate
 3. CMOS Transmission Gate (TG)
- Q.5** (a) Compare FinFET and Planar MOSFET **03**
 (b) Draw transistor level circuit diagram of NOR based SR latch using CMOS. **04**
 (c) What is need of Design of Testability (DFT) in VLSI IC design and explain Built in Self Test (BIST) techniques of DFT **07**
- OR**
- Q.5** (a) Draw and discuss three stage ring oscillator **03**
 (b) Implement and Describe CMOS clocked JK flip-flop **04**
 (c) What is clock-skew? Explain on-chip clock generation and distribution. **07**
