

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER-VI (NEW) EXAMINATION – SUMMER 2024****Subject Code:2161101****Date:22-05-2024****Subject Name:VLSI Technology & Design****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

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| Q.1 | (a) | Compare Semi-custom and Full custom VLSI design style | 03 |
| | (b) | Discuss VLSI design flow in brief | 04 |
| | (c) | Compare constant electric field scaling and constant voltage scaling in detail. | 07 |
| Q.2 | (a) | Explain LOCOS method in detail. | 03 |
| | (b) | Explain the concept of regularity and modularity in brief. | 04 |
| | (c) | Explain MOSFET capacitances in detail. | 07 |
| OR | | | |
| | (c) | Discuss fabrication process of n-channel MOSFET in detail. | 07 |
| Q.3 | (a) | Draw and explain I-V characteristic of nMOS transistor. | 03 |
| | (b) | Explain the channel length modulation effect in detail. | 04 |
| | (c) | Explain MOS system under external bias in detail with suitable energy-band diagrams. | 07 |
| OR | | | |
| Q.3 | (a) | Explain FPGA in brief. | 03 |
| | (b) | Draw and explain the CMOS inverter circuit | 04 |
| | (c) | Draw circuit of nMOS resistive load inverter. Derive V_{IH} , V_{IL} , V_{OL} and V_{OH} for the same. | 07 |
| Q.4 | (a) | What is CMOS ring oscillator? Explain in brief. | 03 |
| | (b) | Explain behavior of bi-stable element in brief. | 04 |
| | (c) | Define the propagation delay τ_{PHL} and τ_{PLH} Derive τ_{PHL} for CMOS inverter. | 07 |
| OR | | | |
| Q.4 | (a) | Prove that switching power dissipation of CMOS inverter is proportional to switching frequency. | 03 |
| | (b) | Explain Generalized NOR structure with Multiple inputs using combinational MOS logic circuits. | 04 |
| | (c) | Derive the threshold voltage expression for CMOS two input NAND Gate. | 07 |
| Q.5 | (a) | Explain controllability and observability in brief. | 03 |
| | (b) | Explain Adhoc testable design technique in brief. | 04 |
| | (c) | Explain voltage Bootstrapping in detail. | 07 |
| OR | | | |
| Q.5 | (a) | Explain Latch-up prevention technique. | 03 |
| | (b) | Write short note on Complimentary pass transistor logic (CPL) | 04 |
| | (c) | Explain Dynamic CMOS Logic (Precharge-Evaluate Logic) in detail. Also illustrate the cascading problem in dynamic CMOS logic. | 07 |
