

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER-VI EXAMINATION – SUMMER 2025

Subject Code:2161101

Date:28-05-2025

Subject Name:VLSI Technology & Design

Time:10:30 AM TO 01:00 PM

Total Marks:70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

- Q.1** (a) Provide a comparative analysis of Semi-custom and Full-custom VLSI design styles. **07**
(b) Explain the behaviour of MOS device under external bias with the help of energy band diagrams and derive the relationship for maximum depletion width at oxide-semiconductor surface. **07**

- Q.2** (a) Explain LOCOS technique used for device isolation and state its advantages over the Etched Field Oxidation technique. **07**
(b) Explain the experimental methods of measuring following parameters of n MOS: Threshold voltage (V_T), channel length modulation coefficient (λ), substrate-bias coefficient (γ), transconductance parameter (k_n) **07**

OR

- (b) Consider a MOS system with the following parameters: **07**
 $t_{ox} = 20 \text{ nm}$
 $\Phi_{GC} = -0.85 \text{ V}$
 $N_A = 2 \times 10^5 \text{ cm}^{-3}$
 $Q_{ox} = q \times 2 \times 10^{11} \text{ C/cm}^2$
(i) Determine the threshold voltage, V_{T0} under zero bias at room temperature ($T = 300 \text{ }^\circ\text{K}$). Consider $\epsilon_{ox} = 3.97\epsilon_0$ and $\epsilon_{Si} = 11.7\epsilon_0$
(ii) Determine the type (p -type or n -type) and amount of channel implant (N_I / cm^2) required to change the threshold voltage to 0.8 V .

- Q.3** (a) Explain resistive load inverter in detail with necessary derivations of V_{OL} , V_{OH} , V_{IL} , V_{IH} . **07**
(b) Explain the MOSFET capacitances in detail. **07**

OR

- Q.3** (a) Describe Elmore Delay technique to estimate the delay of interconnects. **07**
(b) Explain the latch-up problem observed in CMOS circuits and mention various techniques to prevent it. **07**

- Q.4** (a) Draw two-input CMOS NOR and NAND gate circuits. Identify the transistor/s suffering from body bias effect in each of these circuits. Assume single-well CMOS technology **07**
(b) Draw the circuit diagram of a CMOS edge-triggered D-flip-flop and explain. **07**

OR

- Q.4** (a) Discuss the on-chip clock generation and distribution. **07**
(b) Explain the Domino CMOS dynamic logic circuit design in detail. **07**

- Q.5** (a) Explain the basic principles of pass transistor circuits. Also explain logic “0” and logic “1” transfer. **07**
(b) Explain the Built-In-Self-Test (BIST) technique for testing VLSI designs. **07**

OR

- Q.5 (a)** What is the need of voltage bootstrapping? Draw MOSFET based voltage bootstrapping circuit and explain it in detail with mathematical derivations. **07**
- (b)** Write a short note on CMOS Transmission gate. **07**
