

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER-VI (NEW) EXAMINATION – WINTER 2023****Subject Code:2161101****Date:11-12-2023****Subject Name:VLSI Technology & Design****Time:02:30 PM TO 05:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

MARKS

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| Q.1 | (a) Enlist different VLSI design methodologies. And show the impact of different VLSI design styles upon the design cycle time and the achievable circuit performance using graph. | 03 |
| | (b) Define regularity, modularity and locality in context of VLSI design. | 04 |
| | (c) Draw energy band diagram of MOS Structure at surface inversion and derive the expression for threshold voltage. | 07 |
| Q.2 | (a) Draw Y-chart of VLSI Design flow. | 03 |
| | (b) Realize following Boolean logic equation using CMOS inverter. $Z = ((A+B)+CD+E)'$ | 04 |
| | (c) Explain with net sketch diagram nMOSFET fabrication flow. | 07 |
| | OR | |
| | (c) Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA). | 07 |
| Q.3 | (a) Compare static and dynamic logic circuits. | 03 |
| | (b) Draw resistive load inverter and its voltage transfer characteristics. Derive VOL critical voltage equation of resistive load inverter. | 04 |
| | (c) Design a resistive-load inverter with $R_L = 1 \text{ k}\Omega$, such that $V_{OL} = 0.6 \text{ V}$. The enhancement-type nMOS driver transistor has the following parameters $V_{DD} = 5 \text{ V}$, $V_{TO} = 1 \text{ V}$, $\mu_n C_{ox} = 22.0 \text{ }\mu\text{A/V}^2$. Determine the required aspect ratio, W/L of driver transistor. | 07 |
| | OR | |
| Q.3 | (a) Enlist small geometry effects. | 03 |
| | (b) Draw CMOS inverter and its voltage transfer characteristics with mentioning operating region of nMOS and pMOS. Enlist advantages of CMOS inverter. | 04 |
| | (c) Derive VIL critical voltage equation of CMOS inverter. Consider a CMOS inverter circuit with the following parameters: $V_{DD} = 3.3 \text{ V}$, $V_{TON} = 0.6 \text{ V}$, $V_{TOP} = -0.7 \text{ V}$, $k_n = 200 \text{ }\mu\text{A/V}^2$, $k_p = 80 \text{ }\mu\text{A/V}^2$, find the NM_L | 07 |
| Q.4 | (a) Draw CMOS implementation of D latch with two inverters and two CMOS TG gates. | 03 |
| | (b) What is the Scaling? Compare Constant voltage and constant field scaling. | 04 |
| | (c) Derive t_{PHL} propagation delay equation during output high to low transition of CMOS inverter. | 07 |

OR

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| Q.4 | (a) | Draw Ring oscillator circuit using inverters and its output waveform. Write generated frequency equation. | 03 |
| | (b) | Implement 2 inputs multiplexer using 2 Transmission Gates and 1 Inverter. | 04 |
| | (c) | Derive switching power equation of CMOS inverter. | 07 |

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| Q.5 | (a) | What is need of voltage bootstrapping circuit and draw voltage bootstrapping circuit? | 03 |
| | (b) | Implement $F = (A1.A2.A3+B1.B2)'$ using dynamic logic circuit | 04 |
| | (c) | What is latch-up and how to prevent it? | 07 |

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|------------|------------|---|-----------|
| Q.5 | (a) | Draw block diagram of Built in Self Test (BIST). | 03 |
| | (b) | Draw NOR gate based SR latch circuit using CMOS inverter. | 04 |
| | (c) | Discuss the on-chip clock generation and distribution. | 07 |
