

GUJARAT TECHNOLOGICAL UNIVERSITY**BE- SEMESTER-VI (NEW) EXAMINATION – WINTER 2024****Subject Code:2161101****Date:02-12-2024****Subject Name:VLSI Technology & Design****Time:02:30 PM TO 05:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

		MARKS
Q.1	(a) Draw the Gajski-Kuhn Y-chart used for the development of integrated circuits and discuss it in brief.	03
	(b) Compare FPGA and CPLD.	04
	(c) Discuss the LOCOS technique with necessary diagrams.	07
Q.2	(a) Define the symbol V_{IH} and V_{IL} for Inverter and derive the equation of V_{IH} for resistive load inverter.	03
	(b) Explain depletion and inversion region in MOS under external bias.	04
	(c) Calculate the threshold voltage for a polysilicon gate nMOS transistor with the following parameters:	07
	$N_A = 2 \times 10^{16} \text{ cm}^{-3}$, $N_D = 2 \times 10^{19} \text{ cm}^{-3}$, $t_{ox} = 300 \times 10^{-10} \text{ m}$, and $N_{ox} = 10^{10} \text{ cm}^{-2}$, Intrinsic Carrier Concentration of silicon = $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$, Dielectric constant of vacuum = $\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$.	
	OR	
	(c) Consider a CMOS inverter circuit with the following parameters: $V_{DD} = 3.3 \text{ V}$, $V_{TO, n} = 0.6 \text{ V}$, $V_{TO, p} = -0.7 \text{ V}$, $k_n = 200 \mu\text{A/V}^2$, $k_p = 80 \mu\text{A/V}^2$, $k_R = 2.5$ and threshold voltage of nMOS and pMOS are not equal . Calculate the noise margin of the circuit.	07
Q.3	(a) Describe a three-stage ring oscillator circuit with a frequency equation.	03
	(b) For the following Boolean function, $Z = \overline{A(D + E)} + \overline{BC}$, Draw the Stick –diagram layout.	04
	(c) For a CMOS inverter circuit with $V_{DD} = 3.3\text{v}$, $C_{load} = 300 \text{ fF}$, $V_{T, n} = 0.8 \text{ v}$, $V_{GS} = 3.3\text{v}$ the drain characteristic of the nMOS transistor reaches its saturation level at $I_{sat} = 2 \text{ mA}$. Assume input switches instantaneously from 0v to 3.3 v. Using the above data calculate and investigate the delay time necessary for the output to fall from its initial value of 3.3 v to 1.65 v	07
	OR	
Q.3	(a) Explain Noise Immunity and Noise Margin with the necessary diagram.	03
	(b) Design XOR using six transistor and eight transistor CMOS-TG.	04
	(c) Derive the expression for τ_{PHL} using an accurate method for the CMOS inverter.	07

Q.4	(a) Define Scaling. Mention the merits and demerits of constant voltage scaling.	03
	(b) Explain the guideline to avoid Latch-Up.	04
	(c) Discuss pull-down network and pull-up network in CMOS design.	07
OR		
Q.4	(a) Discuss physical, electrical and logical faults observed at Chip Testing.	03
	(b) Illustrate $Z = \overline{(D + E + A)(B + C)}$, Boolean function using CMOS implementation. And find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that $(W/L)_p = 15$ for all pMOS transistors and $(W/L)_n = 10$ for all nMOS transistors.	04
	(c) Discuss CMOS SR latch circuits based on NOR2 gates with the necessary circuit.	07
Q.5	(a) Explain in brief Complimentary pass transistor logic (CPL).	03
	(b) Explain the H-tree Clock distribution network and its purpose.	04
	(c) Explain Voltage bootstrapping in Dynamic logic circuits.	07
OR		
Q.5	(a) Define Controllability and Observability.	03
	(b) Explain CMOS negative (falling) edge-triggered master-slave D flip-flop with the necessary circuit.	04
	(c) Explain Built-in Self-Test (BIST)	07
