

GUJARAT TECHNOLOGICAL UNIVERSITY**BE- SEMESTER-III (NEW) EXAMINATION – WINTER 2024****Subject Code:3132003****Date:29-11-2024****Subject Name: Design Concepts in Basic Electronics****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

- Q.1** (a) Perform binary division of (1101) and (101) and find quotient, remainder and answer. **03**
 (b) Make discrete circuit of AND Gate using TTL. **04**
 (c) Explain No-Bias, Forward Bias and Reverse Bias condition of PN Junction diode. **07**
- Q.2** (a) Write a short note on voltage doubler circuit. **03**
 (b) Compare positive clamper and negative clamper circuits. **04**
 (c) Explain AND, OR, NOT, NAND, NOR, EX-OR and EX-NOR Gates with their symbols and truth tables. **07**
- OR**
- (c) Explain Voltage-Divider Bias Configuration with its application. **07**
- Q.3** (a) Explain D flip-flop with logic diagram and wave forms. **03**
 (b) Briefly explain voltage Tripler and Quadrupler circuits. **04**
 (c) Represent decimal number (-49) as 8-bit sign number using sign bit, 1's complement and 2's complement methods. **07**
- OR**
- Q.3** (a) Convert binary number (110101) to Grey code. **03**
 (b) Explain any one rectifier with circuit diagram and wave forms. **04**
 (c) Explain the operation of 3-bit bidirectional shift register with wave forms. **07**
- Q.4** (a) Write a short note on c-input filter. **03**
 (b) Convert decimal number (96) to binary number by repeated division method. **04**
 (c) Simplify the following Boolean function by means of K-map method and implement the minimized logic using only NAND gates. **07**

$$F(A, B, C, D) = \sum \{1, 2, 3, 5, 8, 9, 11, 13, 14, 15\}$$
- OR**
- Q.4** (a) Give detail comparison of combinational circuits and sequential circuits. **03**
 (b) What is the significant of Q point? **04**
 (c) Simplify the following using Boolean algebra and implement the same using logic gates. $[\{ (A'B)' + C \}' + (ABC)']$ **07**
- Q.5** (a) Briefly explain Emitter Bias Configuration. **03**
 (b) Explain working of Serial In/Parallel Out shift register. **04**
 (c) Design and explain working of 4-bit Decoder. **07**
- OR**
- Q.5** (a) Briefly explain minterms and maxterms in K-map. **03**
 (b) Explain working of any two parallel clipper circuits. **04**
 (c) What is the significance of digital counter? Explain working of 3-bit synchronous counter. **07**
