

Enrollment No./Seat No.:

GUJARAT TECHNOLOGICAL UNIVERSITY
Bachelor of Engineering - SEMESTER - III EXAMINATION - WINTER 2025

Subject Code: BE03041011

Date: 15-12-2025

Subject Name: Digital Electronics

Time: 10:30 AM TO 01:00 PM

Total Marks: 70

Instructions

- 1. Attempt all questions.**
- 2. Make suitable assumptions wherever necessary.**
- 3. Figures to the right indicate full marks.**
- 4. Simple and non-programmable scientific calculators are allowed.**

	Marks
Q.1 (a) Convert the following numbers: (i) $(582.75)_{10}$ to Binary and Hexadecimal (ii) $(3A7.FD)_{16}$ to Octal and Decimal	03
(b) State and prove De Morgan's theorem for two variables using truth table.	04
(c) Implement the Boolean function $F = AB + BC + AC$ using basic logic gates and verify with truth table.	07
Q.2 (a) Define the following parameters: (i) Propagation Delay (ii) Fan-out (iii) Noise Margin	03
(b) Simplify the following Boolean expression using Boolean algebra: $F = A'B'C + A'BC + AB'C + ABC$	04
(c) Design a full adder circuit. Draw the logic diagram, truth table, and write the Boolean expressions for Sum and Carry.	07
OR	
(c) Design a full subtractor circuit. Draw the logic diagram, truth table, and write the Boolean expressions for Difference and Borrow.	07
Q.3 (a) Differentiate between combinational and sequential circuits with suitable examples.	03
(b) Simplify the following Boolean function using 3-variable K-map: $F(A,B,C) = \sum m(0, 1, 3, 5, 7)$	04
(c) Design a 2-bit synchronous UP counter that counts the sequence 0, 1, 2, 3, and repeats. Use JK flip-flops. Show the state diagram, excitation table, K-maps for J & K inputs, and the final logic diagram.	07

OR

- (a) Explain the working of 4:1 multiplexer with logic diagram and truth table. 03
- (b) Simplify the following Boolean function using 3-variable K-map: 04
 $F(A,B,C) = \sum m(0, 2, 4, 6, 7)$

- (c) Explain the working of a 4-bit binary Ripple Counter. Draw the logic diagram using JK flip-flops (with $J=K=1$) and a corresponding timing diagram showing the output waveforms. 07

- Q.4** (a) Explain the working of D flip-flop with circuit diagram and truth table. 03
- (b) Design a 2-to-4 line decoder using basic logic gates. Draw the logic diagram and truth table. 04
- (c) Explain R-2R ladder type Digital to Analog Converter with neat diagram. 07

OR

- (a) Explain the working of JK flip-flop with circuit diagram and truth table. 03
- (b) Design a 4:1 multiplexer using basic logic gates. Draw the logic diagram and truth table. 04
- (c) Explain successive approximation type Analog to Digital Converter with block diagram. 07

- Q.5** (a) Explain the architecture of Programmable Array Logic (PAL) with suitable diagram. Mention its advantages and limitations. 03
- (b) Explain the working of a 4-bit ripple counter with timing diagram. 04
- (c) Design a 3-bit even parity generator circuit. Draw the truth table and implement using logic gates. 07

OR

- (a) Explain the architecture of Programmable Logic Array (PLA) with suitable diagram. Compare it with PAL. 03
- (b) Explain the working of a 4-bit shift register with block diagram. 04
- (c) Design a 2-bit magnitude comparator. Derive the truth table and implement using logic gates. 07
