Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–II • EXAMINATION – SUMMER-2018

Subject Code: 2720314 **Date: 23/05/2018**

Subject Name: Advanced VLSI Design

Time:02:30 PM TO 05:30 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw the timing diagram observed while simulating the design of x^4 implementation of Pipe line architecture in Xilinx ISE that shows all signalsobserved in simulation window and justifies functionality of the design. Statethroughput, latency and timing of your design with proper justification.	**07**
	(b)	Write a verilog program of 16-to-1 multiplexer using conditional operator	**07**
Q.2	**(a)**	Design and write Verilog HDL code for negative edge sensitive S-R flip-flop.	**07**
	(b)	Write verilog code of the 8-bit universal shift register.	**07**
		OR	
	(b)	Explain Register Balancing for timing in Architecting Speed.	**07**
Q.3	**(a)**	How design end and fork join block differs in execution? Explain with example along with waveforms.	**07**
	(b)	Design 4-bit synchronous counter. Use UDP JK Flipflop.	**07**
		OR	
Q.3	**(a)**	Draw the circuit of 32x1 multiplexer using 8x1 multiplexer, 2 to 4 decoder and basic gates. Write Verilog program for 32x1 multiplexer using structural modeling. Write Verilog modules for 8x1 mux, 2 to 4 decoder and required basic gates also.	**14**
Q.4	**(a)**	Implement the Function $Y= AX^4+ BX^3+CX^2+DX$ in Verilog considering maximum time delay in the critical path of one 8 bit x 8 bit multiplier delay only. Assume A,B,C,D,E,X, and Y of 8 bit. Draw implementation diagram of the same. What is the throughput and latency of your design?	**14**
		OR	
Q.4	**(a)**	Consider Moore Finite State Machine (FSM) with one input X and one output Z. The FSM asserts its output Z when it recognize the "1010" input bit sequence. Implement the state diagram for above and write Verilog code for it.	**14**
Q.5	**(a)**	Write verilog code to design a 4-bit adder using full adder and half adder. Use gate level modeling for half and full adders. Show synthesized output of your design.	**14**
		OR	
Q.5	**(a)**	With the help of T flip flop design 4 bit decade counter. Show all design steps. Write Verilog program of the same using structural modeling style. Also write Verilog program of the all components used in your design.	**14**

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