Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**ME – SEMESTER – I (New) EXAMINATION – WINTER 2018**

**Subject Code: 2710507** **Date: 12-Dec-2018**

**Subject Name: ASIC Design**

**Time: 10:30 AM To 01:00 PM** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | List the major capabilities of VHDL along with the features that differentiate it from other hardware description languages. | **07** |
| | **(b)** | Explain various operators in detail for VHDL. | **07** |
| **Q.2** | **(a)** | Explain basic data types in VHDL. | **07** |
| | **(b)** | Write a VHDL code for Full Adder using dataflow.<br>Write a VHDL code for 4 bit binary parallel adder using generate statement.<br>Use Full Adder as component. | **07** |
| | | **OR** | |
| | **(b)** | Write the VHDL code for JK Flip-flop. Consider preset and clear as direct inputs. | **07** |
| **Q.3** | **(a)** | Write VHDL listing for 3X8 Decoder with enable signal facility. | **07** |
| | **(b)** | Explain Process Statement. Explain importance of Sensitivity List in process statement with example. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Write a VHDL code for 4x1 MUX using<br>(1) IF… Else statement<br>(2) Case statement. | **07** |
| | **(b)** | What is VHDL Test Bench? Explain with simple example | **07** |
| **Q.4** | **(a)** | Explain following terms with reference to VHDL<br>(1) Exit Statement<br>(2) Wait Statement<br>(3) Generic | **07** |
| | **(b)** | Define Mealy State Machine and Moore State Machine. Compare them | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | Draw and Explain FPGA Architecture | **07** |
| | **(b)** | Explain configuration and package declaration statements using necessary examples. | **07** |
| **Q.5** | **(a)** | Explain ASIC design flow in flow with necessary block diagram | **07** |
| | **(b)** | Write VHDL code for 1011 sequence detector using FSM. | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | What do you understand by Delta – Delay? Also explain Inertial Delay Model and Transport Delay Model. | **07** |
| | **(b)** | Explain ROM, PAL, PLA, and PLD. | **07** |

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